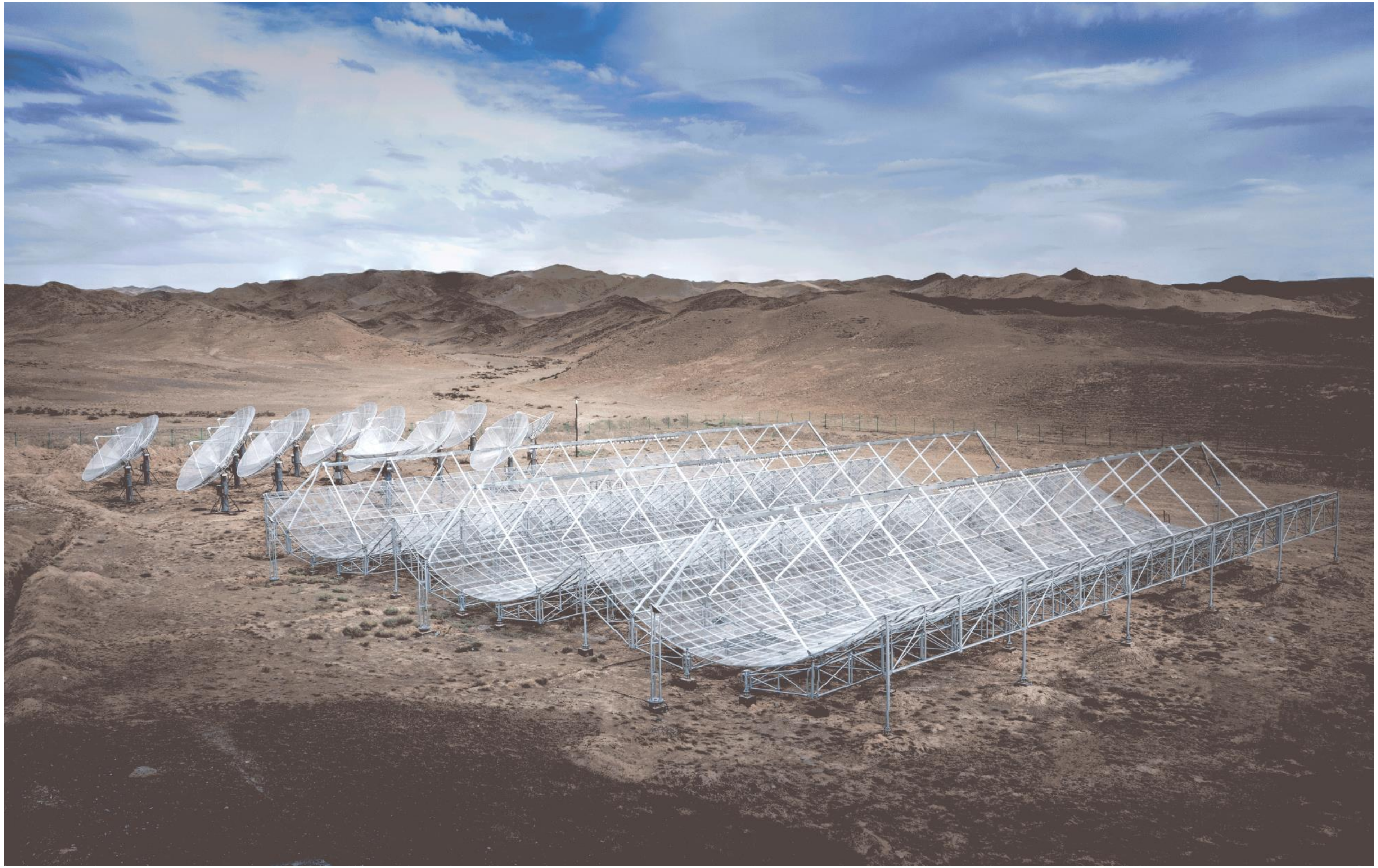
A Scalable Digital Correlator Based on ROACH2+GPU Cluster for Tianlai 96-Dual-Polarization Antenna Array

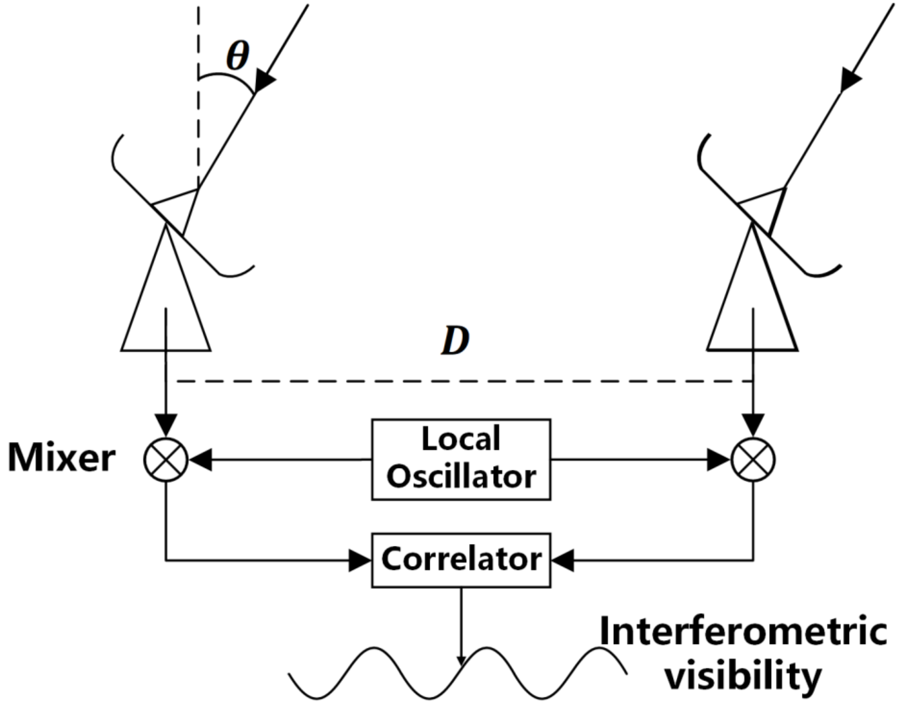
Zhao Wang

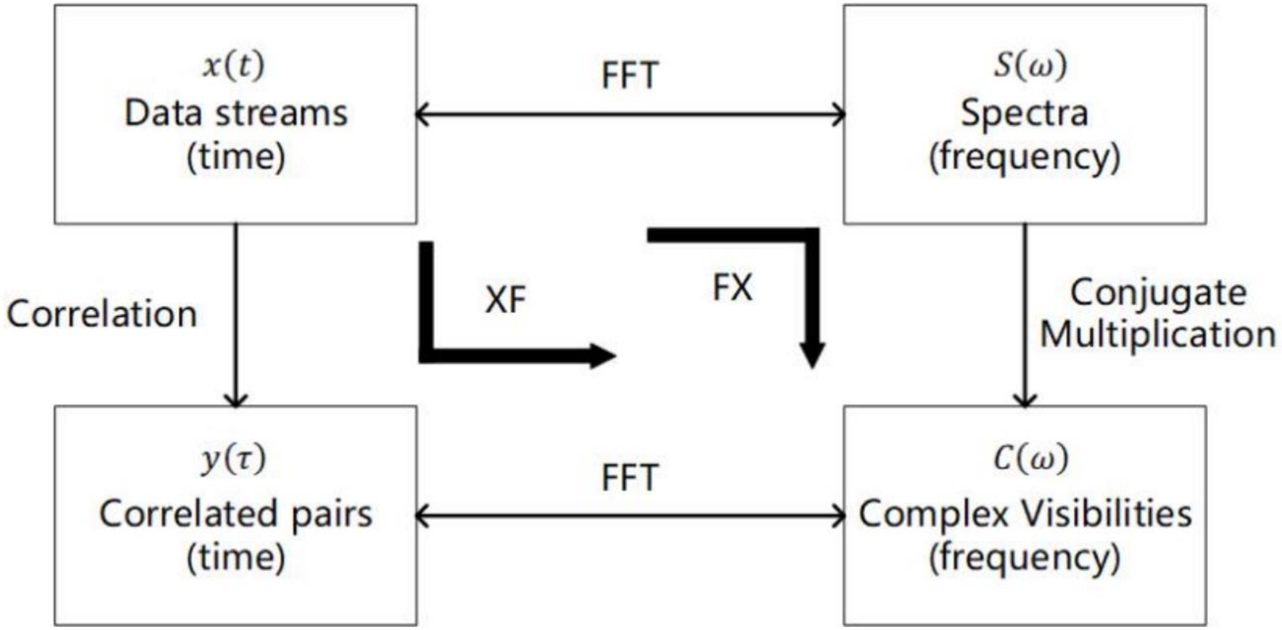
Collaborators：Ke Zhang，Jixia Li，Fengquan Wu，Haijun Tian，Chenhui Niu，Qunxiong Wang

Tianlai Pathfinder Array

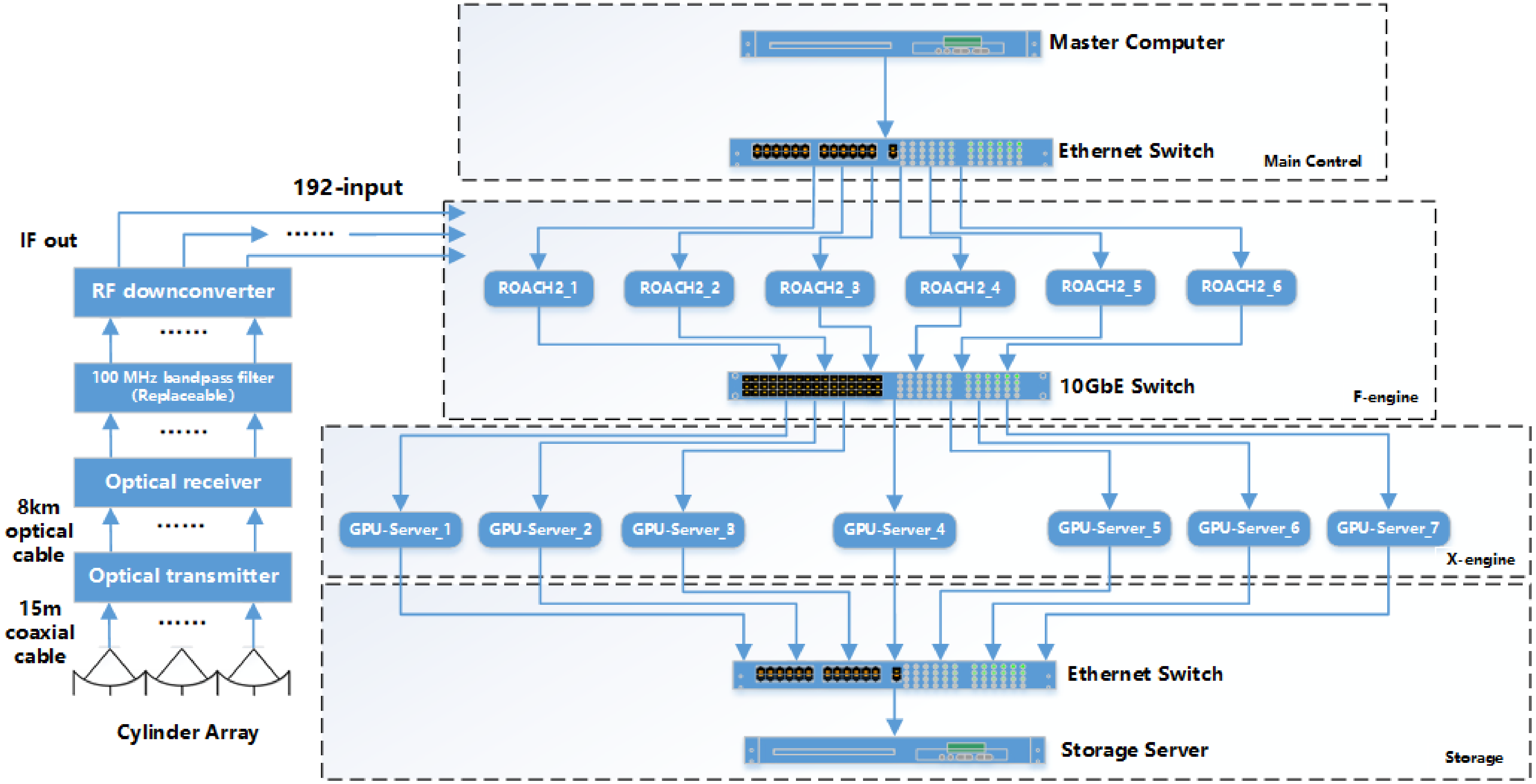


What is a Correlator?



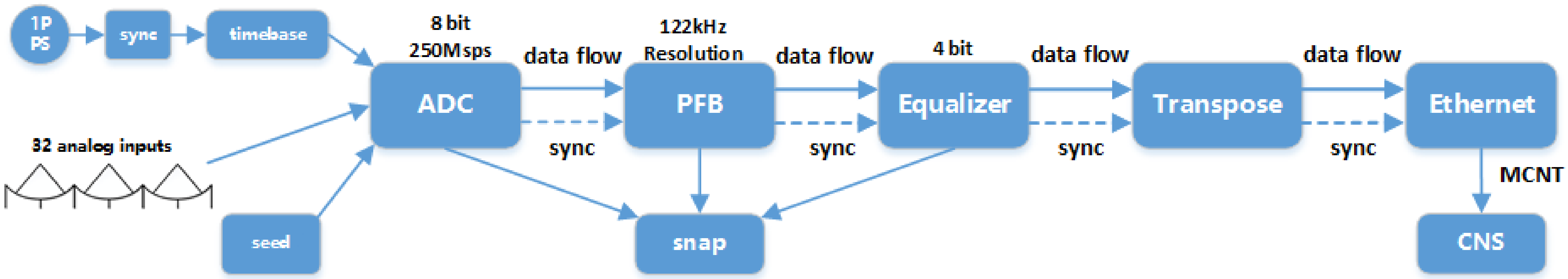


Correlator System

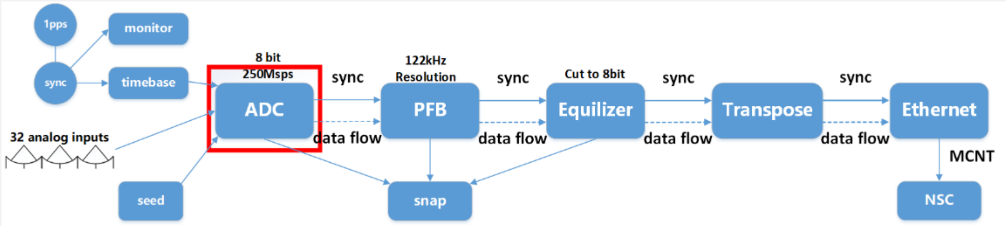


Master Computer
Ethernet Switch
Main Control
192-input
IF out
RF downconverter
ROACH2_1
ROACH2_2
ROACH2_3
ROACH2_4
ROACH2_5
ROACH2_6
10GbE Switch
F-engine
100 MHz bandpass filter (Replaceable)
Optical receiver
8km optical cable
GPU-Server_1
GPU-Server_2
GPU-Server_3
GPU-Server_4
GPU-Server_5
GPU-Server_6
GPU-Server_7
X-engine
Optical transmitter
15m coaxial cable
Ethernet Switch
Storage Server
Storage
Cylinder Array

F-engine Data Flow



ADC



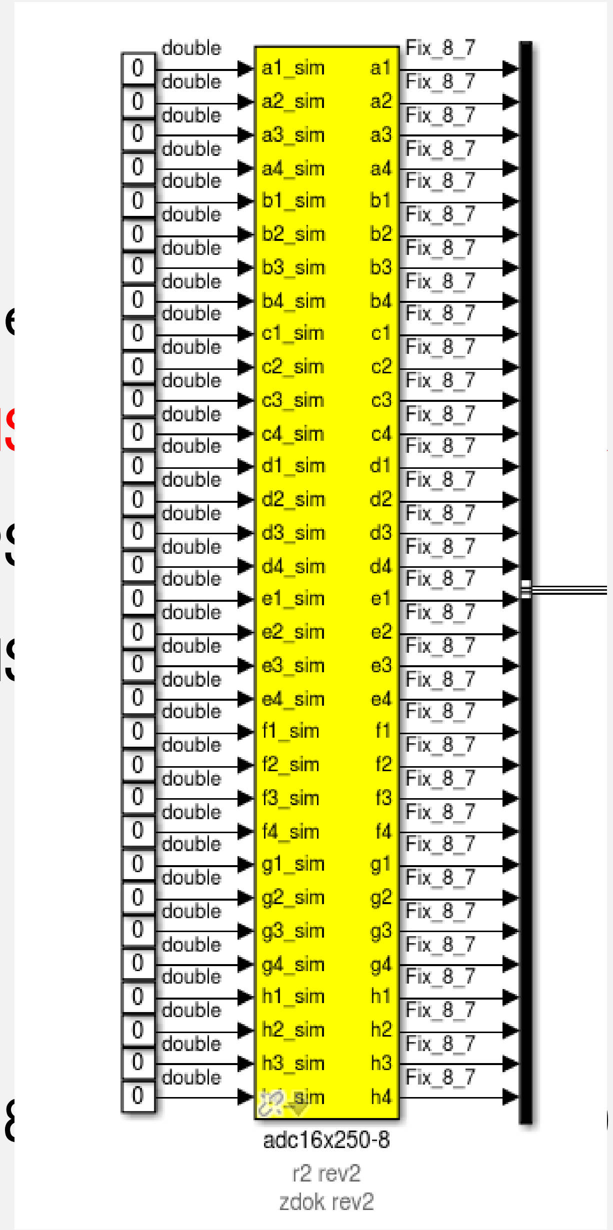
1） ADC16x250-8

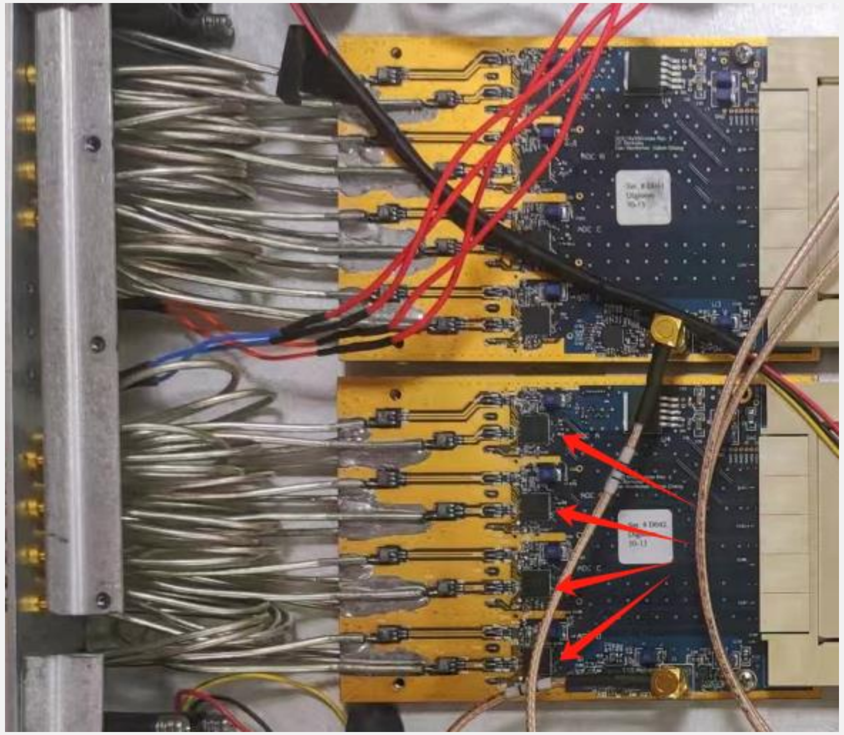
run time programmable ope

16 inputs by 250 MS ult)

8 input by 500 MSPS

4 inputs by 1000 MS



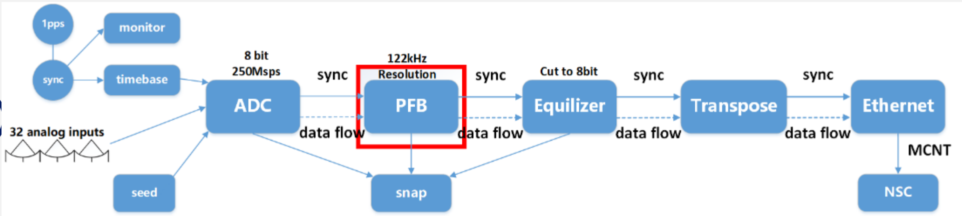


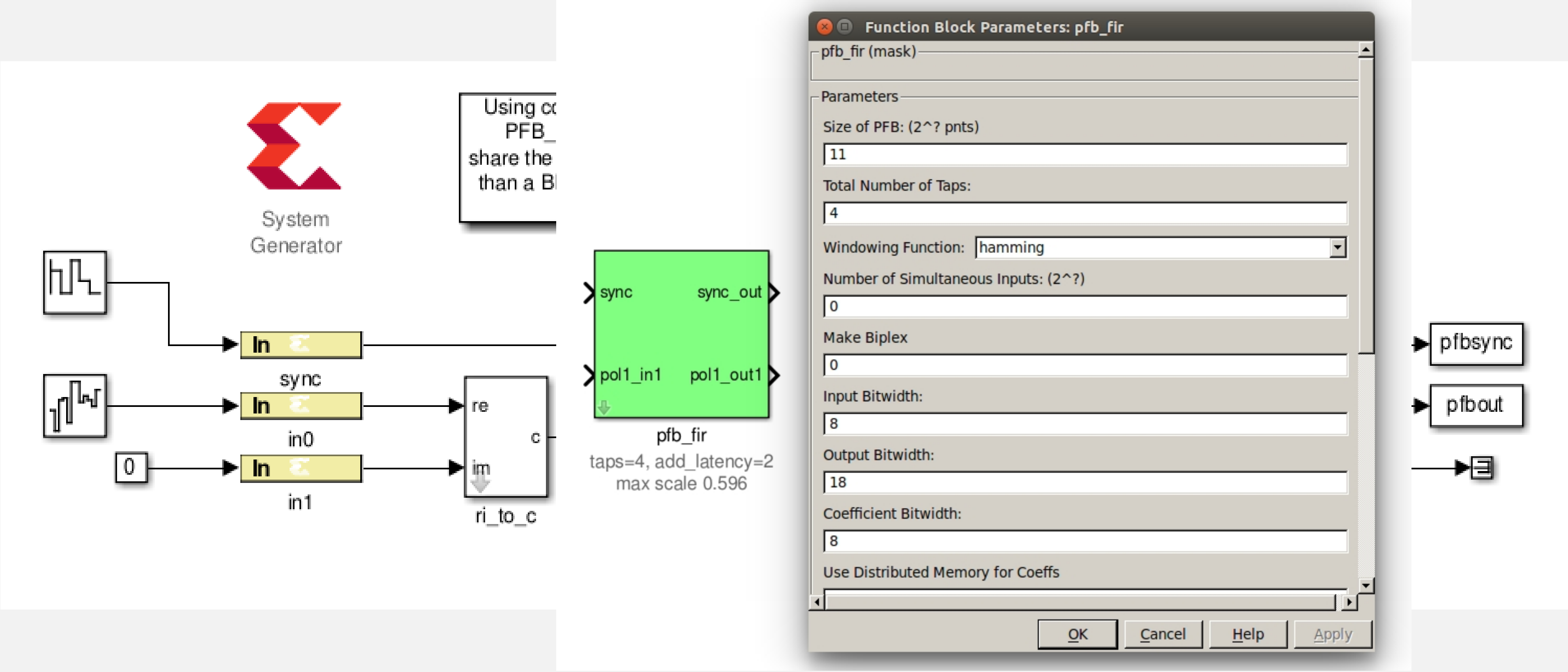
4 x HMCAD1511

Selectable gain factor

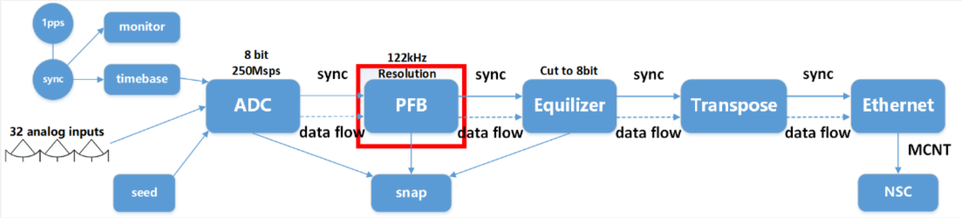
[1、1.25、2、2.5、4、5、8 、25、32、50]

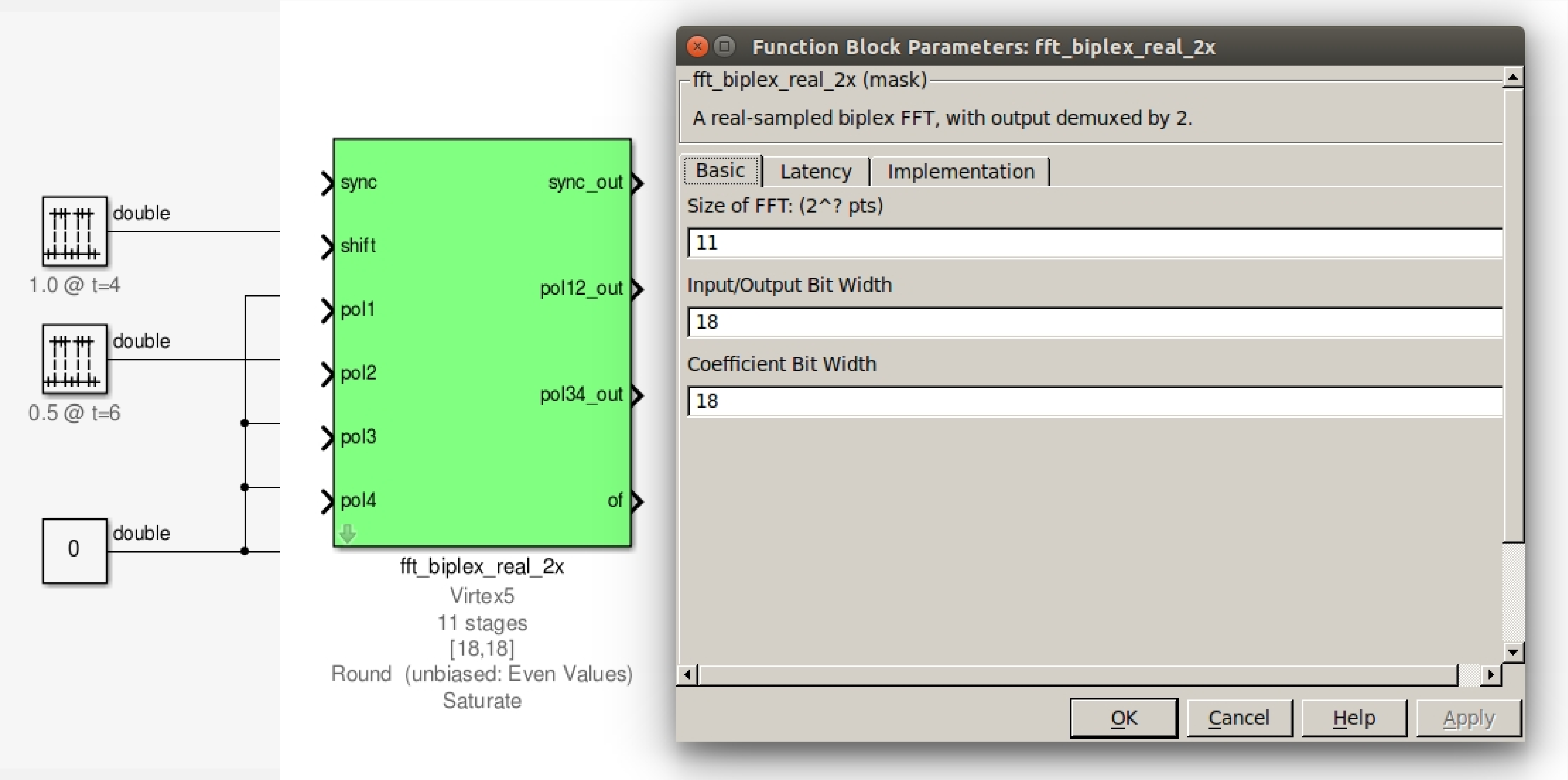
PFB : Polyphase FIR Filter Frontend



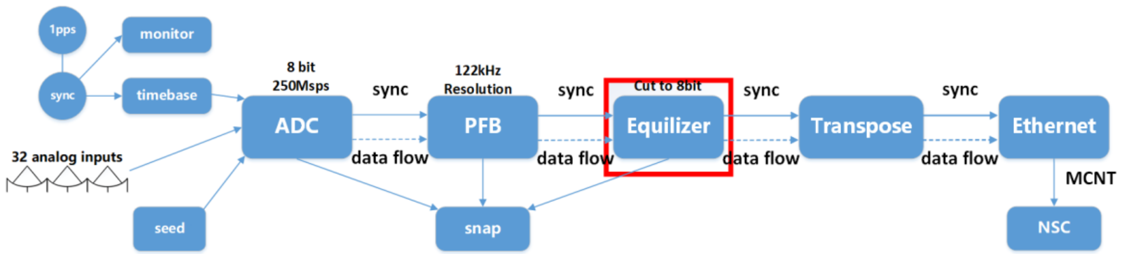


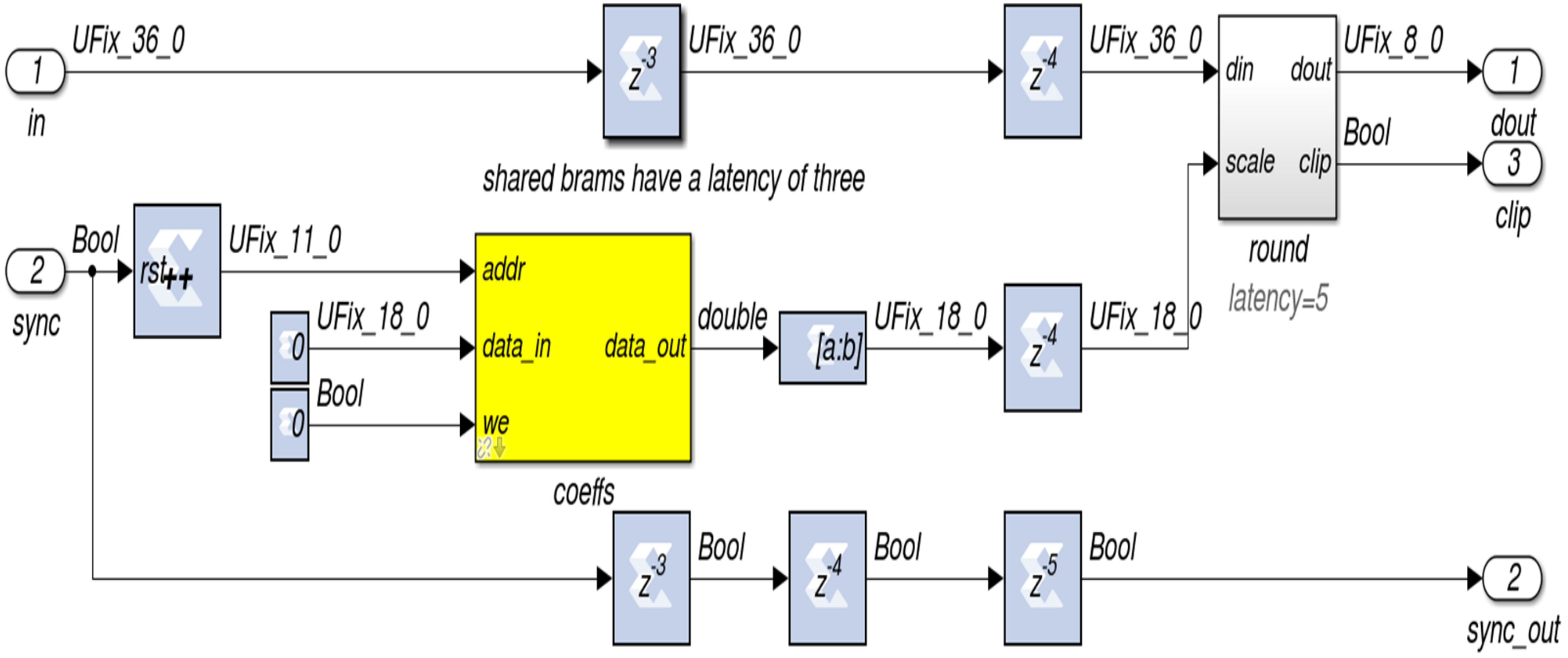
PFB : FFT


1pps
monitor
sync
timebase
8 bit
250Msps
ADC
sync
122kHz
Resolution
PFB
sync
Cut to 8bit
Equilizer
sync
Transpose
sync
Ethernet
32 analog inputs
data flow
data flow
data flow
data flow
MCNT
seed
snap
NSC

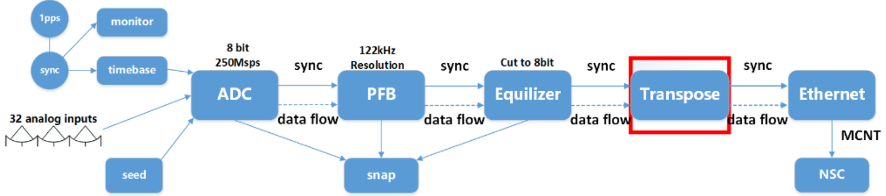

double
1.0 @ t=4
double
0.5 @ t=6
0
double
sync
shift
pol1
pol2
pol3
pol4
sync_out
pol12_out
pol34_out
of
fft_biplex_real_2x
Virtex5
11 stages
[18,18]
Round (unbiased: Even Values)
Saturate
Function Block Parameters: fft_biplex_real_2x
fft_biplex_real_2x (mask)
A real-sampled biplex FFT, with output demuxed by 2.
Basic
Latency
Implementation
Size of FFT: (2^? pts)
11
Input/Output Bit Width
18
Coefficient Bit Width
18
OK
Cancel
Help
Apply

Equalizer

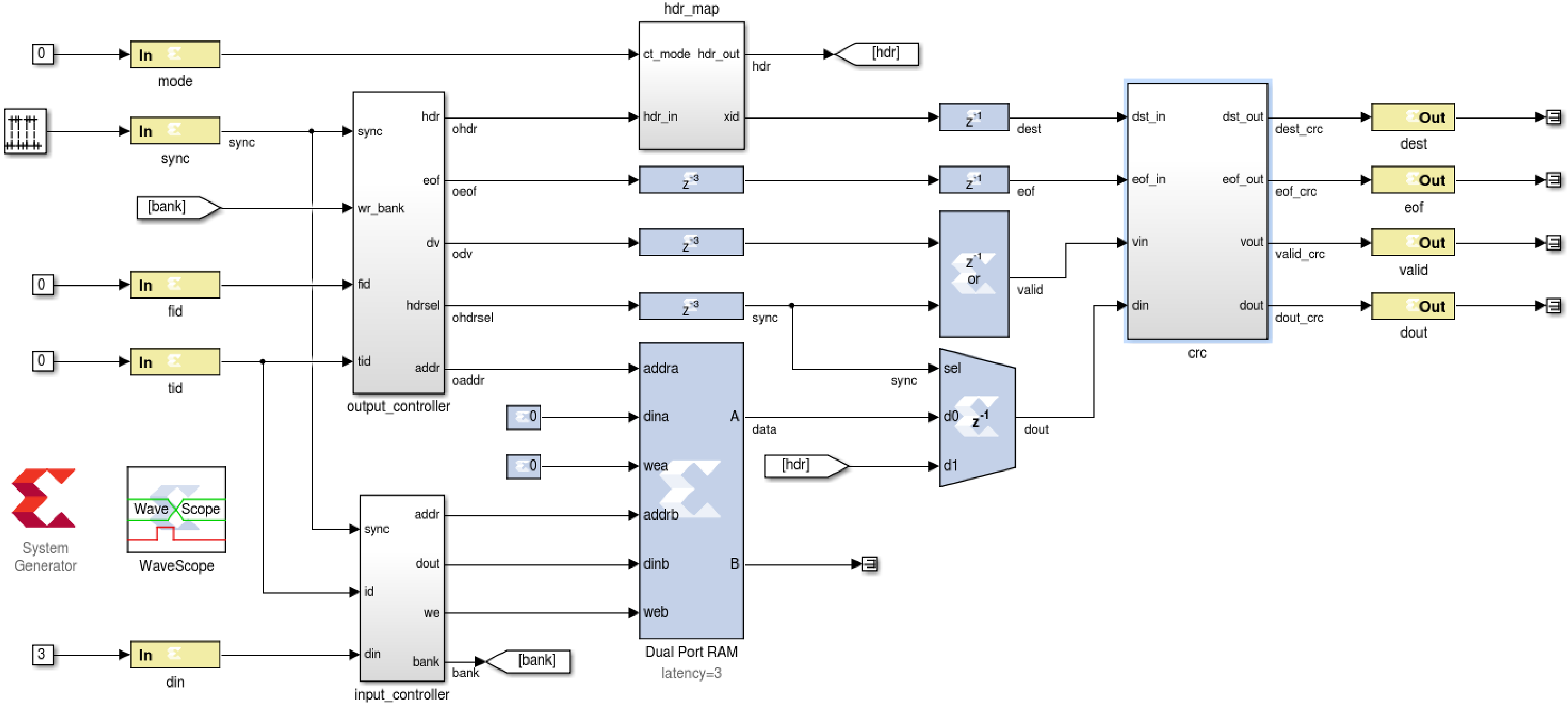

1pps
monitor
sync
timebase
32 analog inputs
seed
8 bit
250Msps
ADC
sync
data flow
122kHz
Resolution
PFB
sync
data flow
Cut to 8bit
Equilizer
sync
data flow
Transpose
sync
data flow
Ethernet
MCNT
NSC
snap


1
in
UFix_36_0
z-3
UFix_36_0
shared brams have a latency of three
z-4
UFix_36_0
din
dout
scale
clip
round
latency=5
UFix_8_0
1
dout
Bool
3
clip
2
sync
Bool
rst
++
UFix_11_0
addr
UFix_18_0
0
data_in
Bool
0
we
data_out
coeffs
double
[a:b]
UFix_18_0
z-4
UFix_18_0
z-3
Bool
z-4
Bool
z-5
Bool
2
sync_out

Transpose

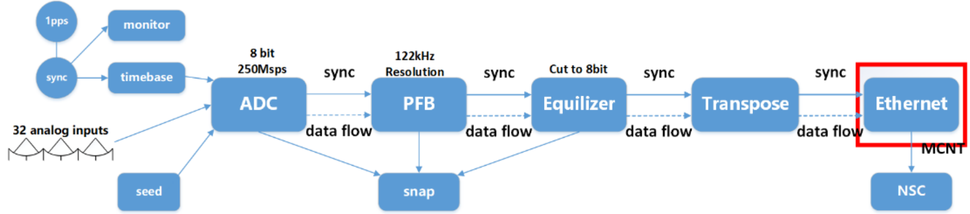


1pps
monitor
sync
timebase
32 analog inputs
seed
8 bit 250Msps
ADC
sync
data flow
122kHz Resolution
PFB
sync
data flow
Cut to 8bit
Equilizer
sync
data flow
Transpose
sync
data flow
Ethernet
MCNT
NSC
snap



hdr_map
mode
sync
[bank]
fid
tid
din
output_controller
input_controller
ohdr
oeof
odv
ohdrsel
oaddr
ct_mode hdr_out
hdr_in xid
hdr
[hdr]
dest
eof
valid
sync
data
dout
Dual Port RAM
latency=3
addra
dina
wea
addrb
dinb
web
sel
d0
d1
dst_in dst_out
eof_in eof_out
vin vout
din dout
crc
dest_crc
eof_crc
valid_crc
dout_crc
Out
dest
eof
valid
dout
System Generator
WaveScope
bank

Ethernet



1pps
monitor
sync
timebase
8 bit
250Msps
ADC
sync
122kHz
Resolution
PFB
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Cut to 8bit
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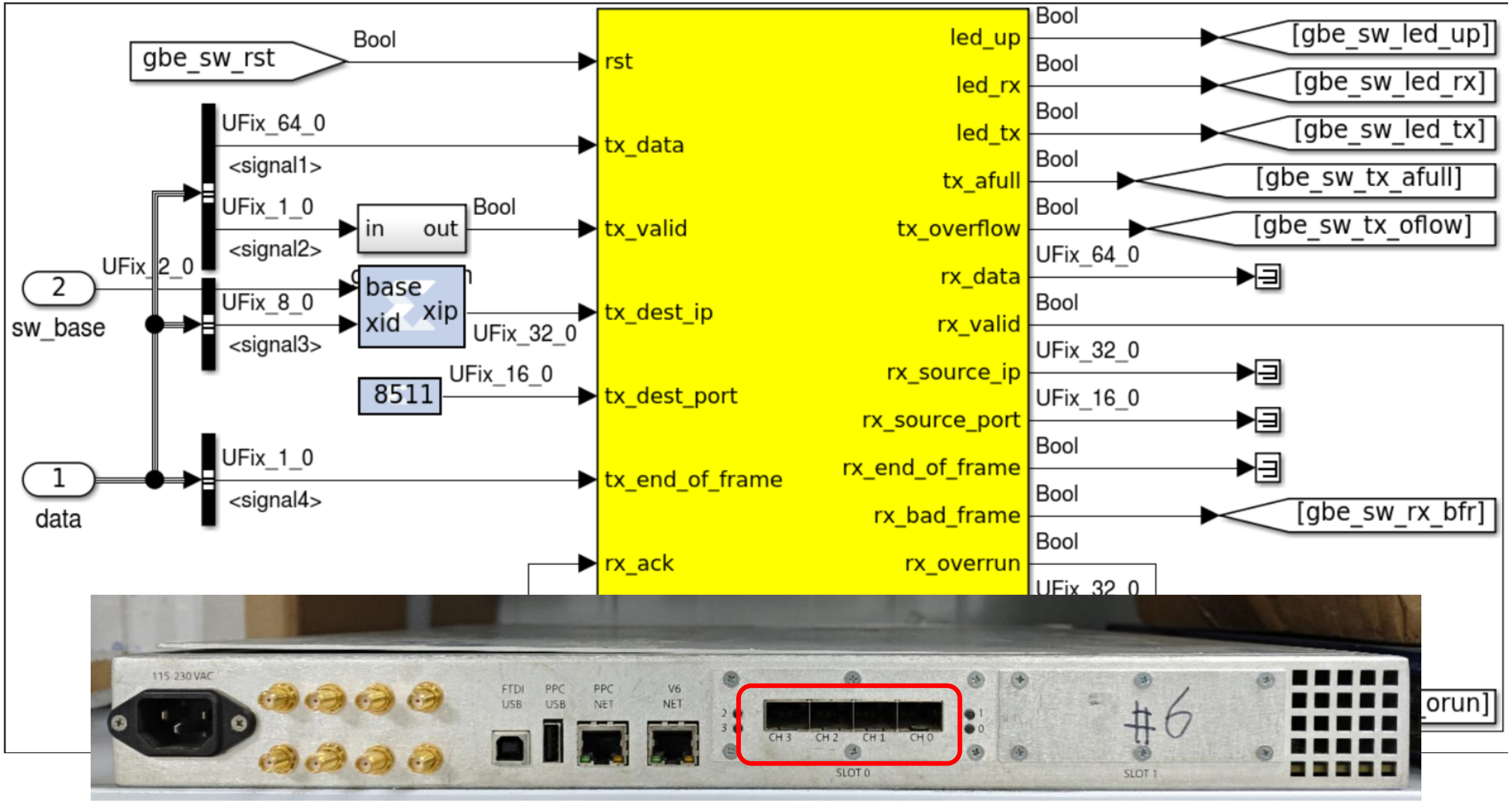
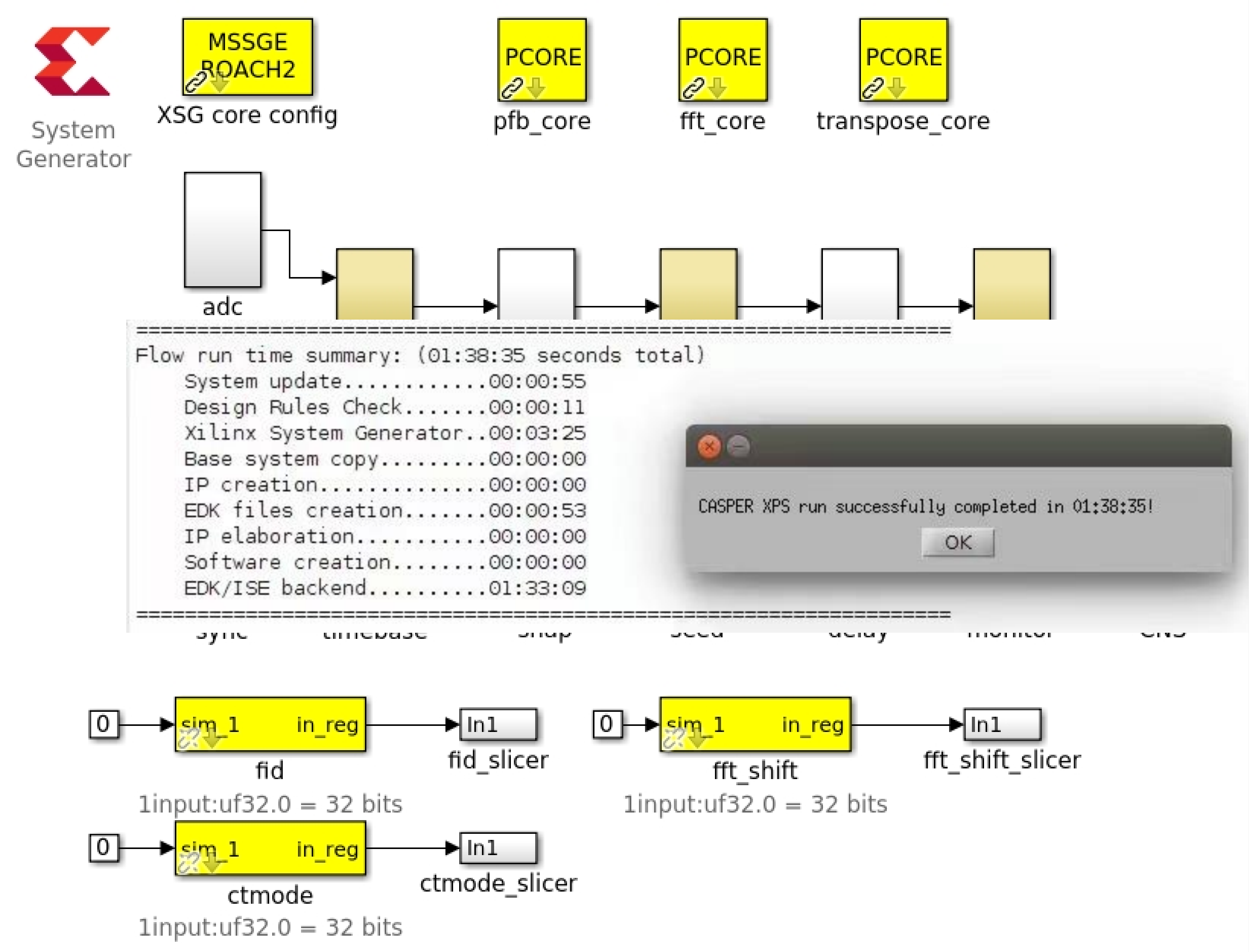
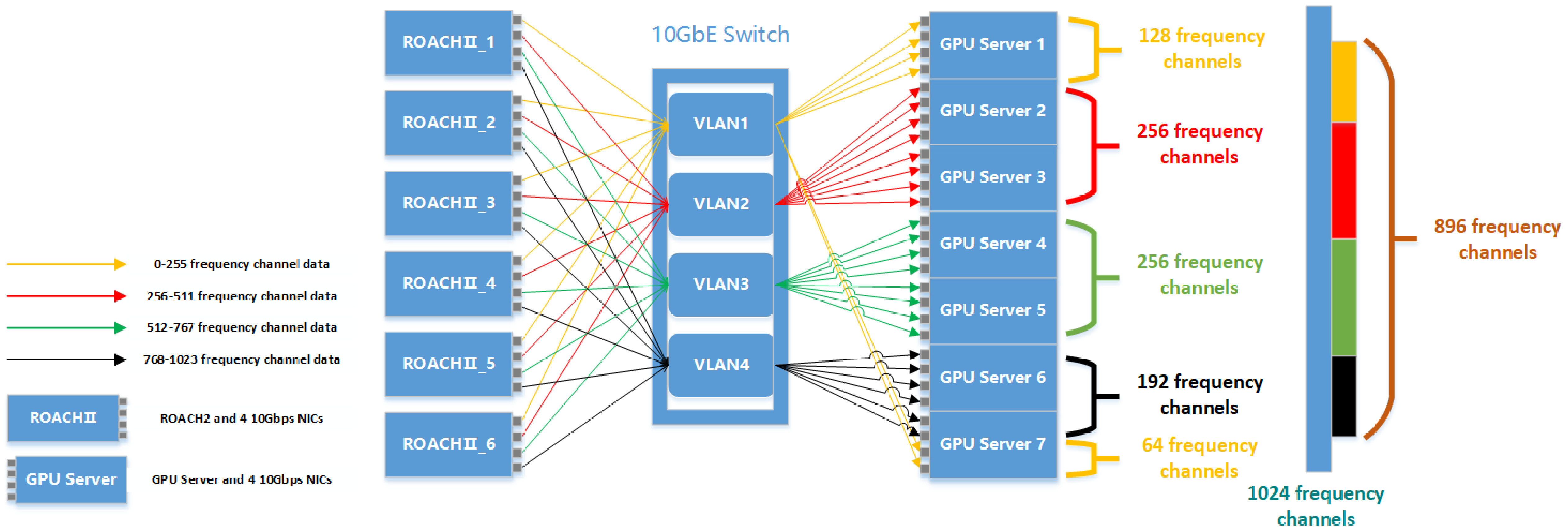


gbe_sw_rst
Bool
rst
UFix_64_0
<signal1>
tx_data
UFix_1_0
<signal2>
in out
Bool
tx_valid
UFix_2_0
2
sw_base
UFix_8_0
<signal3>
base
xid
xip
UFix_32_0
tx_dest_ip
8511
UFix_16_0
tx_dest_port
1
data
UFix_1_0
<signal4>
tx_end_of_frame
rx_ack
led_up
led_rx
led_tx
tx_afull
tx_overflow
rx_data
rx_valid
rx_source_ip
rx_source_port
rx_end_of_frame
rx_bad_frame
rx_overrun
Bool
Bool
Bool
Bool
Bool
UFix_64_0
Bool
UFix_32_0
UFix_16_0
Bool
Bool
Bool
UFix_32_0
[gbe_sw_led_up]
[gbe_sw_led_rx]
[gbe_sw_led_tx]
[gbe_sw_tx_afull]
[gbe_sw_tx_oflow]
[gbe_sw_rx_bfr]
orun]
115-230 VAC
FTDI
USB
PPC
USB
PPC
NET
V6
NET
CH 3
CH 2
CH 1
CH 0
SLOT 0
#6
SLOT 1

Software Platform MATLAB、Simulink、System generator、EDK



Network

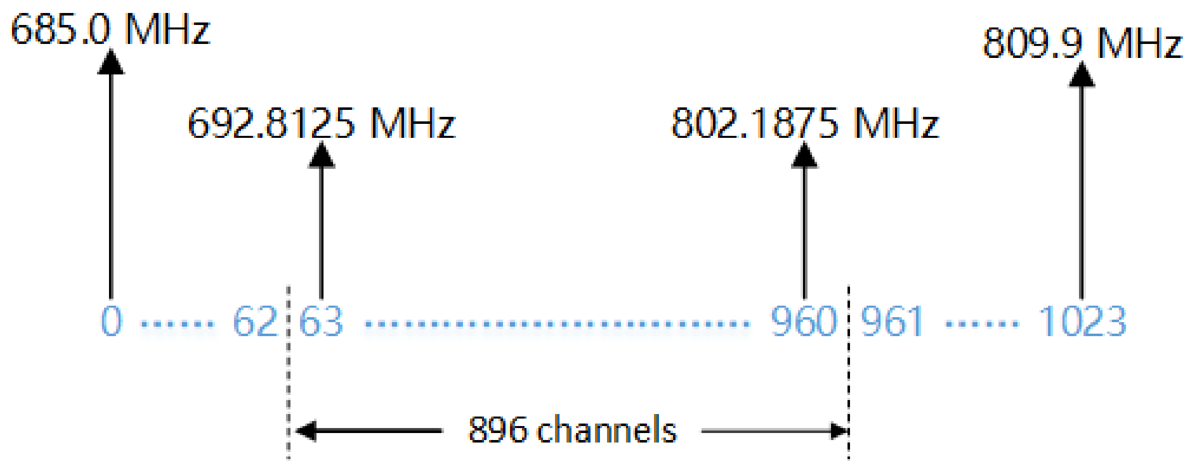


0-255 frequency channel data
256-511 frequency channel data
512-767 frequency channel data
768-1023 frequency channel data
ROACHII
ROACH2 and 4 10Gbps NICs
GPU Server
GPU Server and 4 10Gbps NICs
ROACHII_1
ROACHII_2
ROACHII_3
ROACHII_4
ROACHII_5
ROACHII_6
10GbE Switch
VLAN1
VLAN2
VLAN3
VLAN4
GPU Server 1
GPU Server 2
GPU Server 3
GPU Server 4
GPU Server 5
GPU Server 6
GPU Server 7
128 frequency channels
256 frequency channels
256 frequency channels
192 frequency channels
64 frequency channels
896 frequency channels
1024 frequency channels

Network

- Signal bandwidth: 125 MHz
- Effective bandwidth :100 MHz
- Frequency range: 700 MHz – 800 MHz
- ADC sample rate: 250 Msps
- Number of frequency channels: 1024
- Frequency resolution:

$$\Delta\upsilon = 125\ \mathrm{MHz}/1024 = 122.07\ \mathrm{kHz}$$



- Signal bandwidth handled by each GPU server:

$$128 \times 122.07\mathrm{kHz} = 15.625\ \mathrm{MHz}$$

- Seven GPU servers(896 frequency channels):

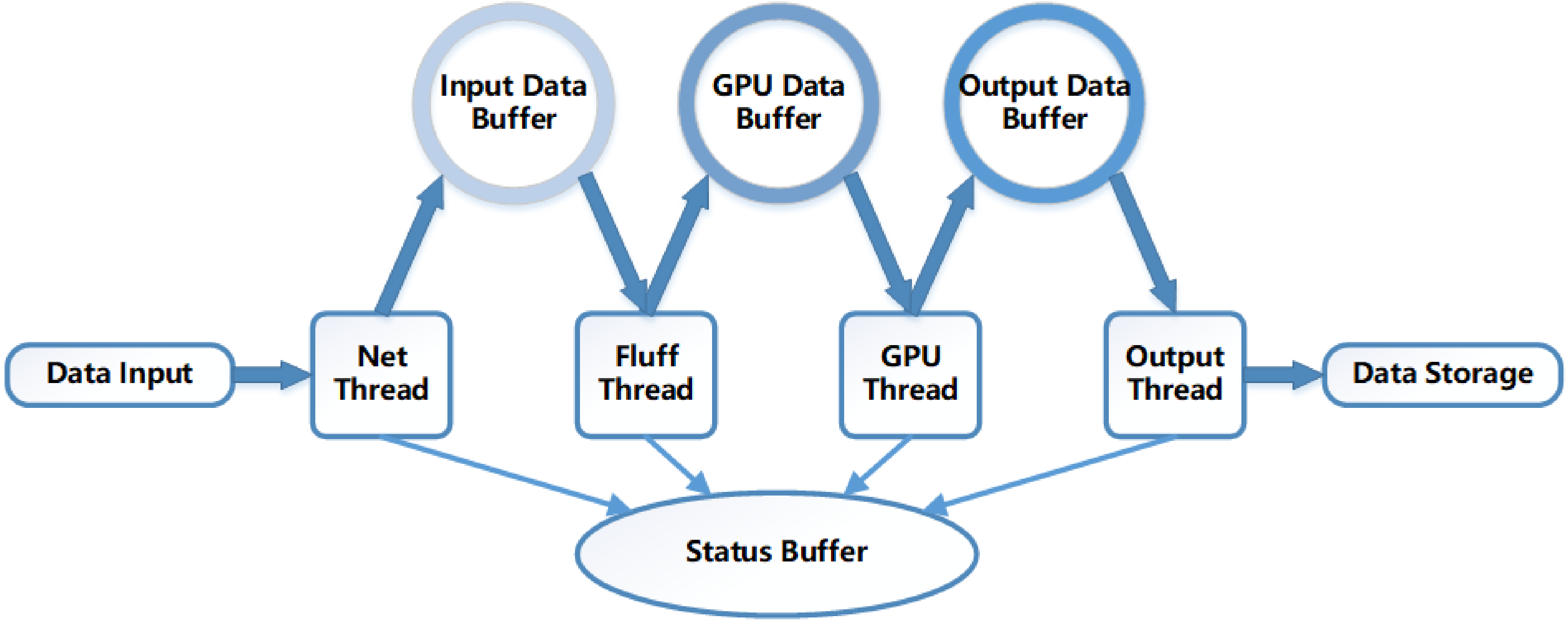
$$15.625\mathrm{MHz} \times 7 = 109.375\ \mathrm{MHz} > 100\ \mathrm{MHz}$$ (effective bandwidth)

X-engine： Hardware

Work lead by Zhang Ke

Hardware	Processor	Graphics card	NIC	PCIe	Memory
Supermicro	Dual Intel E5-2670	Dual GTX 690	Dual 2-port 10GbE	3.0	128 GB RAM
Dell	Dual Intel E5-2699	One RTX 3080	Dual 2-port 10GbE	4.0	256 GB RAM

X-engine：Hashpipe （High Availibility Shared Pipeline Engine）



The data operation in the X-engine is managed by the hashpipe software running on CPU and GPU heterogeneous servers.

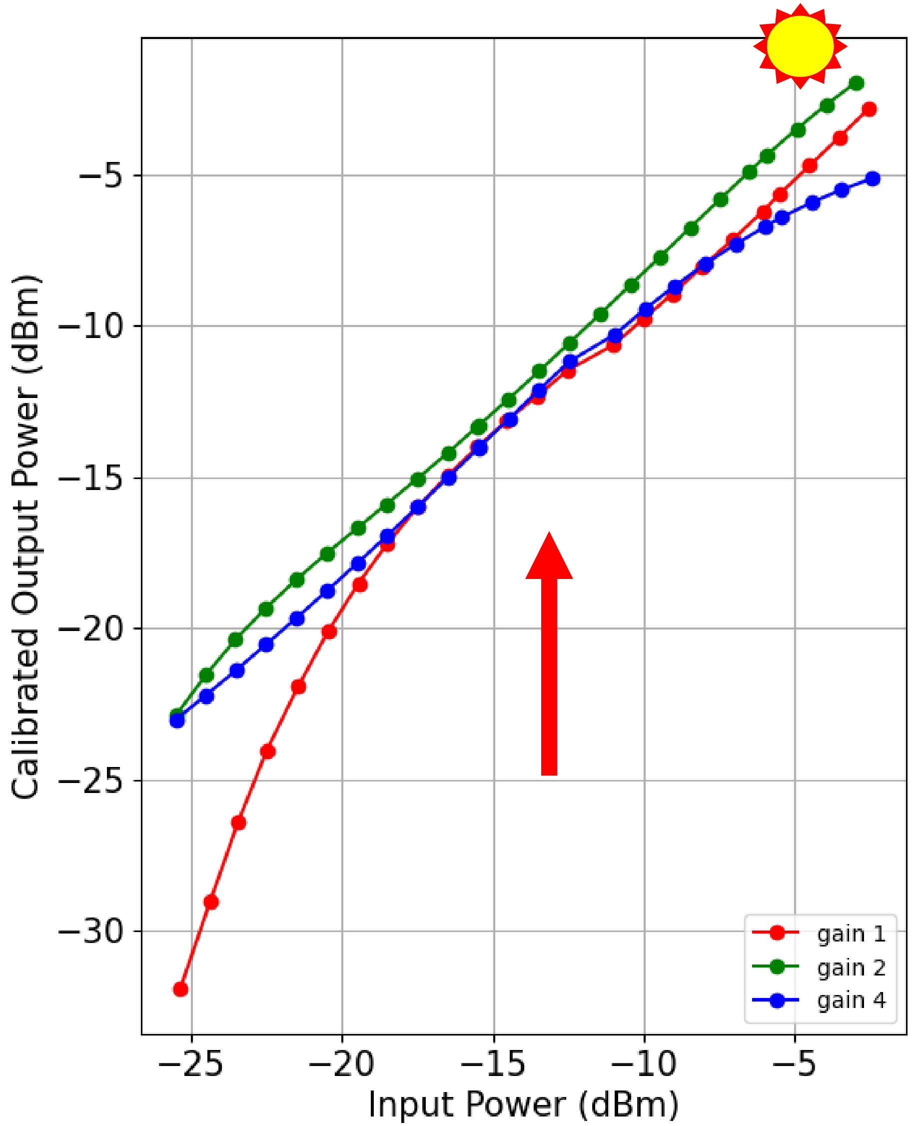
Hashpipe was originally developed as an efficient shared pipe engine for the National Astronomical Observatory, the Universal Green Bank Astrospectrograph (Prestage et al. 2009).

The GPU CMAC is done by xGPU which is written by M.Clerk (Clark et al., 2013).

Cluster Correlator Linearity

IF output level is adjusted to about -13dB mW.

ADC gain : 2



Correlator system’s linear dynamic range is between -22 dBm and 0 dBm within the 125 MHz bandpass.

In real observations, the power levels from the receivers vary by at most 10 dB, so this dynamic range meets the observation needs.

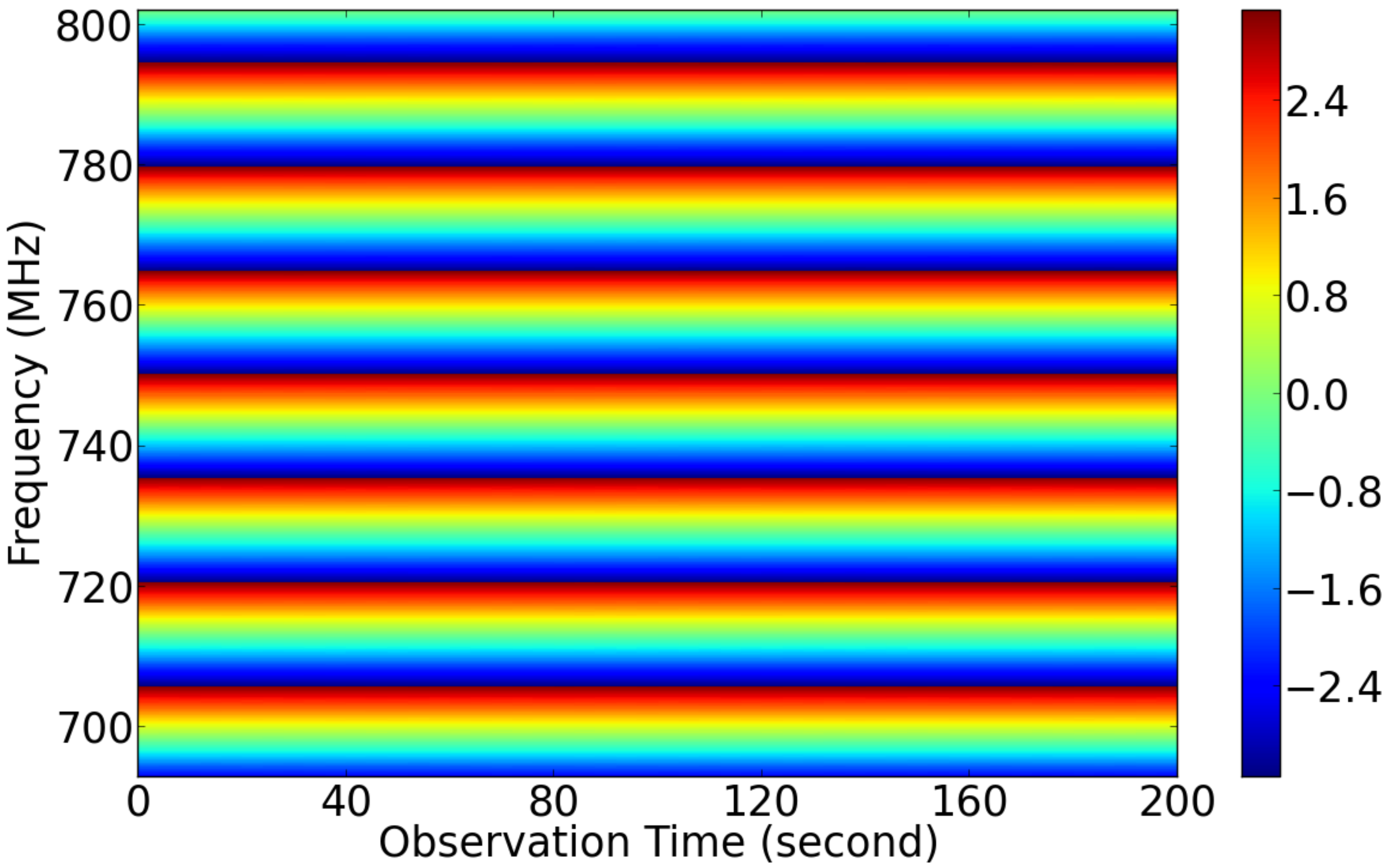
Phase Calculation Accuracy Test

$S_1 = A_1 e^{i(2\pi f t + \phi_0)}$

$S_2 = A_1 e^{i(2\pi f (t+\tau) + \phi_0)}$

$V = \langle S_1^* \cdot S_2 \rangle = A_1 A_2 e^{i 2\pi f \tau}$

$\Phi = 2\pi\tau f$

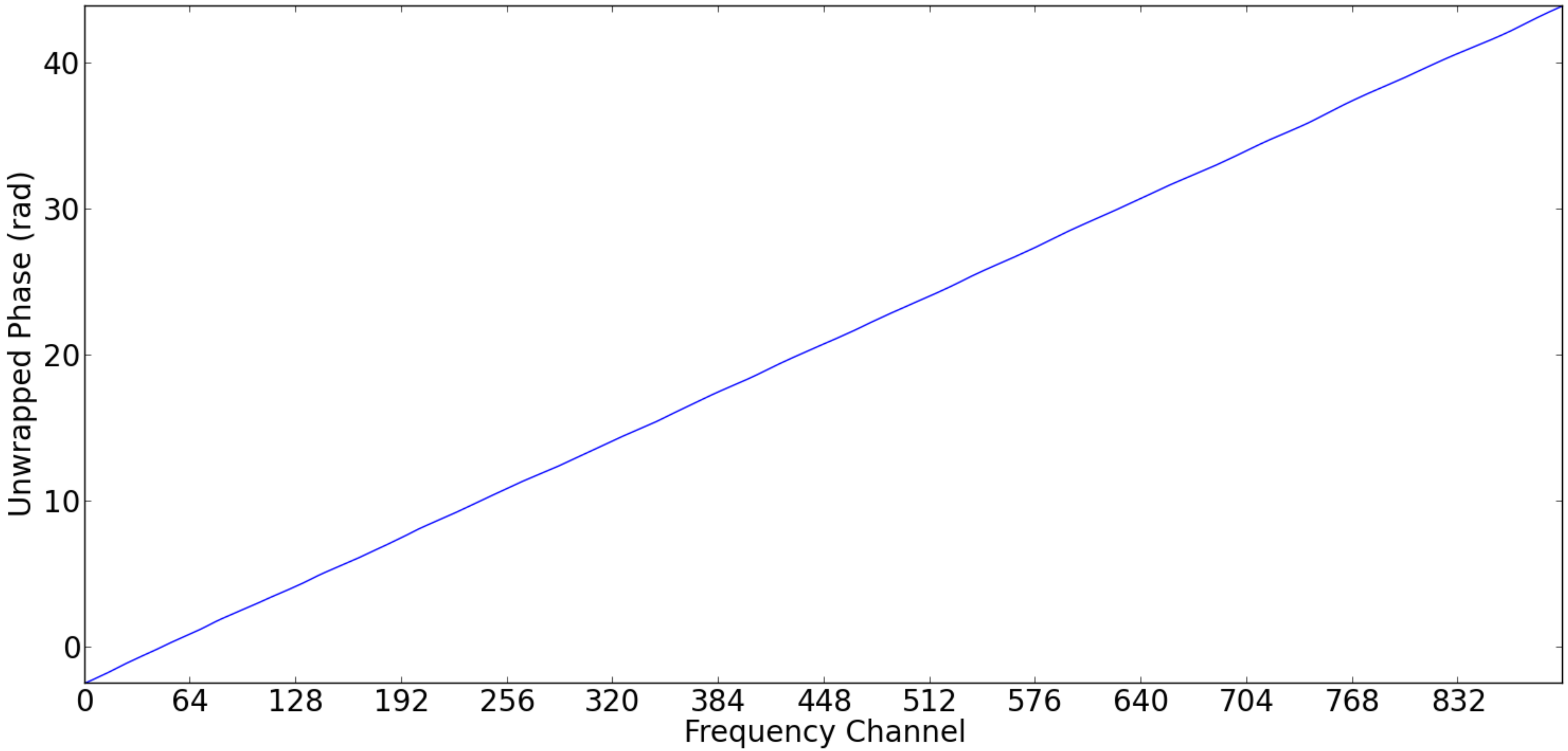


Phase Calculation Accuracy Test

$$k = 2\pi\tau$$

$$\tau = \Delta l / \tilde{c}$$

$$\Delta l = 15m$$



we obtain a propagation speed in the coaxial cable of about 0.78c (0.78 times speed of light in vacuum), which is consistent with the specification of the RF cable.

Power

Six ROACH2 Boards + Master Computer : 220 V x 3.5 A = 770 W

Seven GPU Servers + 10GbE Switch + 1GbE Switch : 220 V x 17.5 A = 3850 W

Total power: ： 770 W + 3850 W = 4620 W

Thank you for your attention!