Paon4 : a testbench for Idrogen boards

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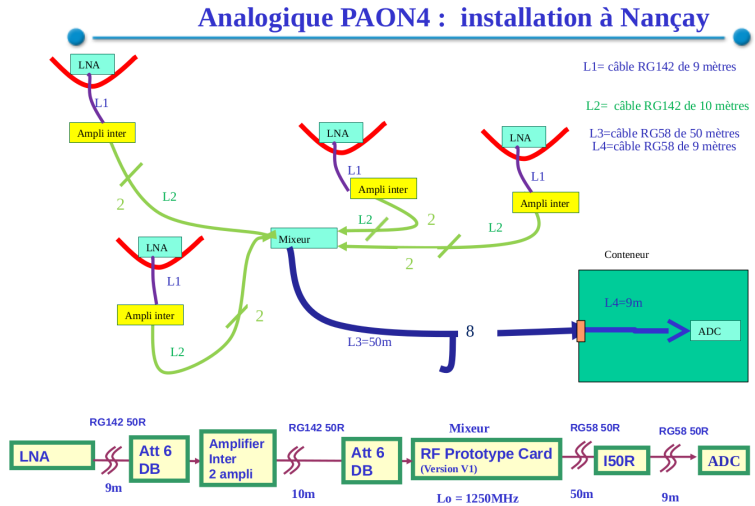
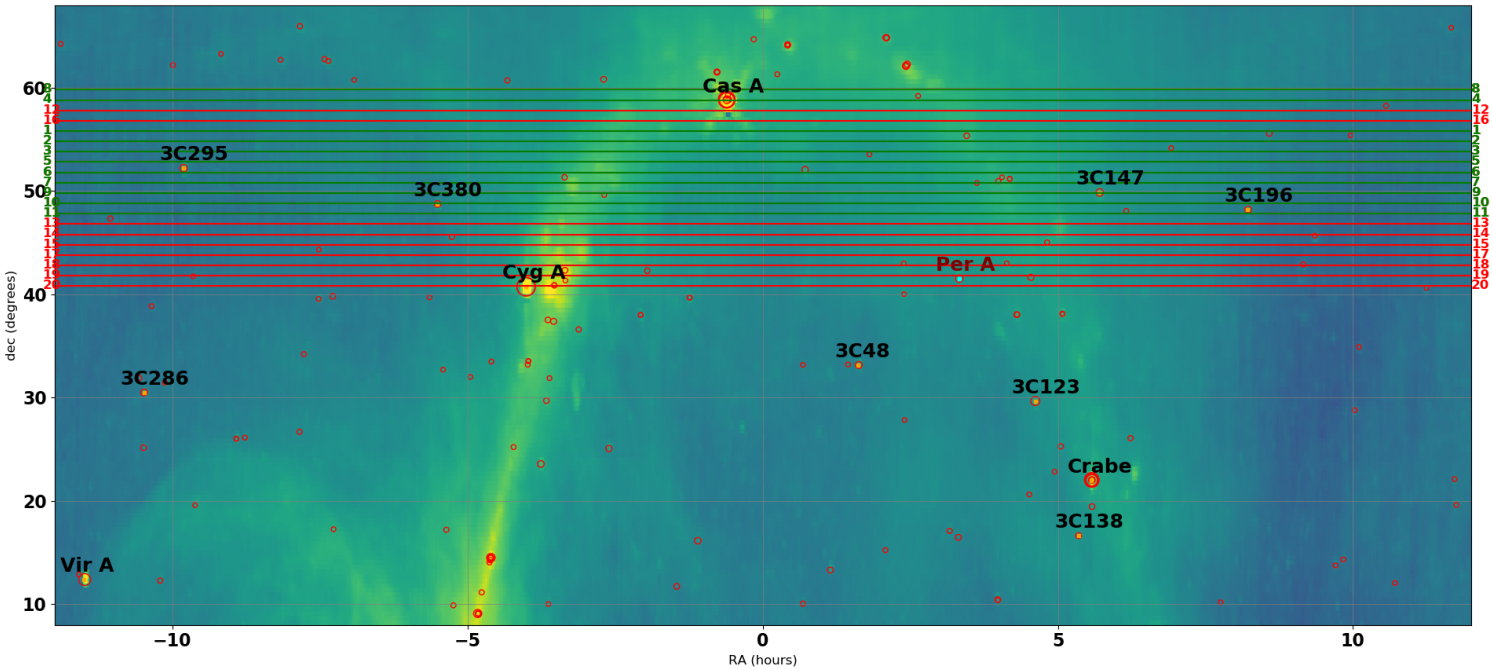
PAON4

Collaboration between LAL (now IJCLab, Orsay), Obs. de Paris (Meudon, Nançay), IRFU/CEAEA (Saclay)
Characteristics :

- 4 antennas ($\varnothing$=5m, $\sim 3 deg^2$ FOV) in Nançay ($\sim$ 200 km south of Paris)
- 2 polar./antenna
- Frequency band 1250 - 1500 MHz ($\sim$ 1275 - 1480 MHz fiducial)
- transit observations e.g. $\sim$ 24h scans
- $\pm$ 20 degrees from zenith
- test bench for electronics, DAQ, on-line computing, analysis
- R.Ansari et al., MNRAS 493 (2020) 2, 2965
- live-time $\sim$ 10%



PAON4 operations



- 2014-8 : building, tests and upgrades (blind channel for calibration)
- 2017-8 : fight against a systematic perturbation (bird's effect)
- 2018-9 : regular observations 24h ⟼ 1 week
  - check complex gain stability
  - determination of geometry + phases with GNSS satellites

Main systematics

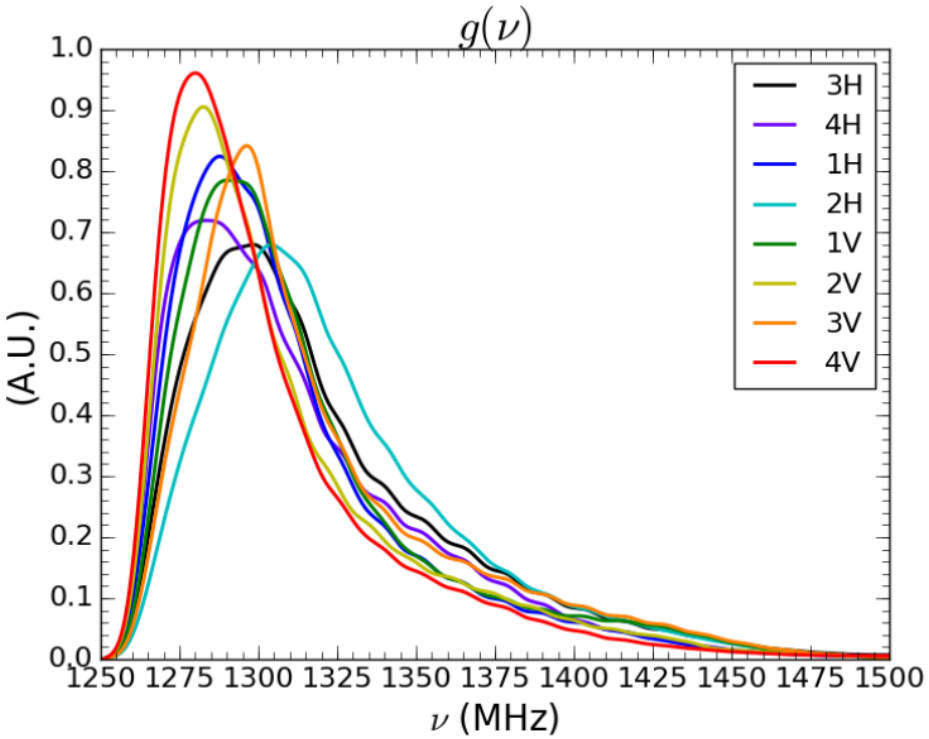
- wide bandwidth (250 MHz)
- frequency translation with LO
- long coaxial connexions 10+10+50m

⇒ impedance adaptation mismatch(es)

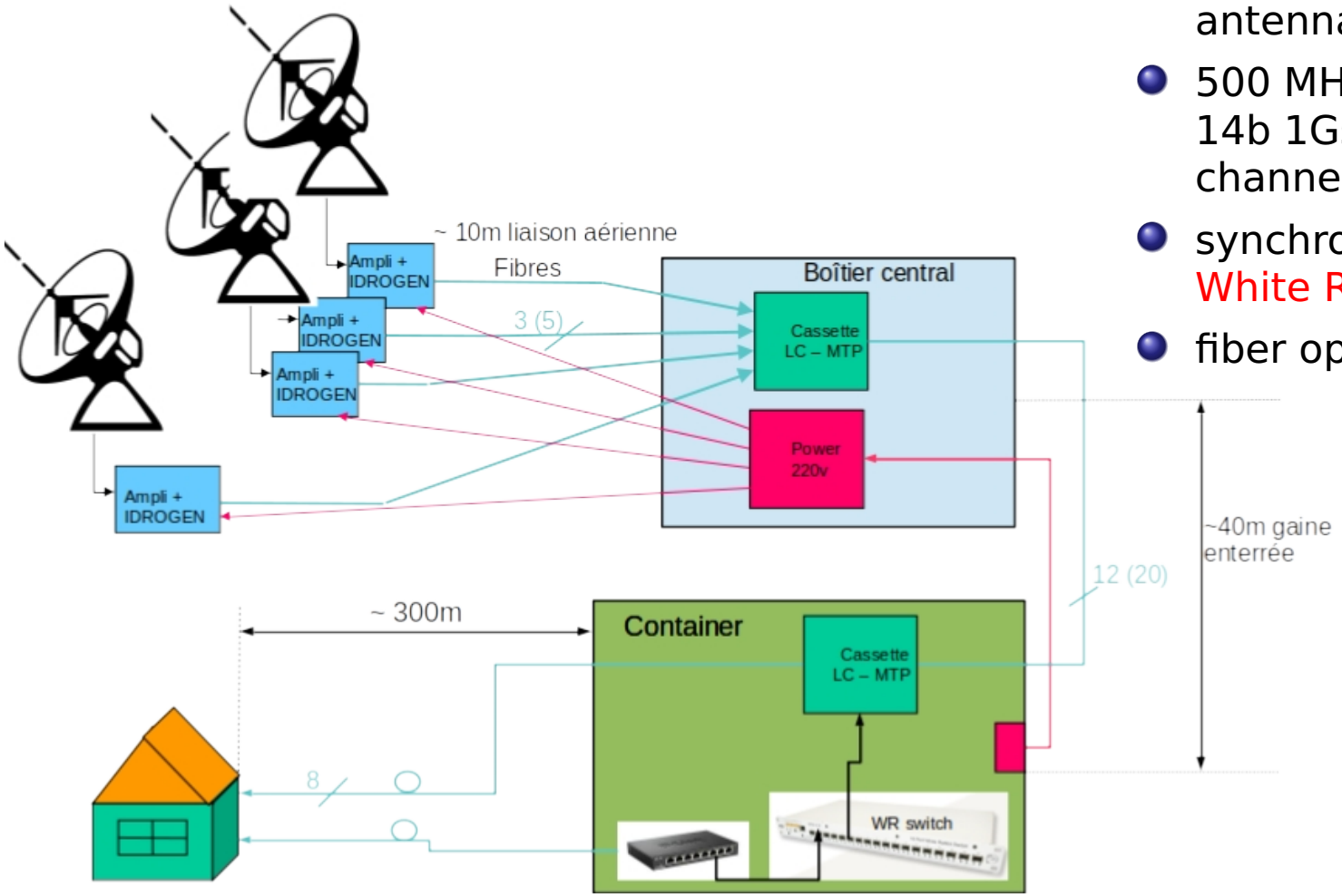
⇒ standing waves in the cable(s) (time/condition dependent)

- to improve on this : digitize on the antennas with IDROGEN boards
- ⇒ avoid systematics from transport of broad band analog signal(s) on long distances

Frequency responses of PAON4 channels

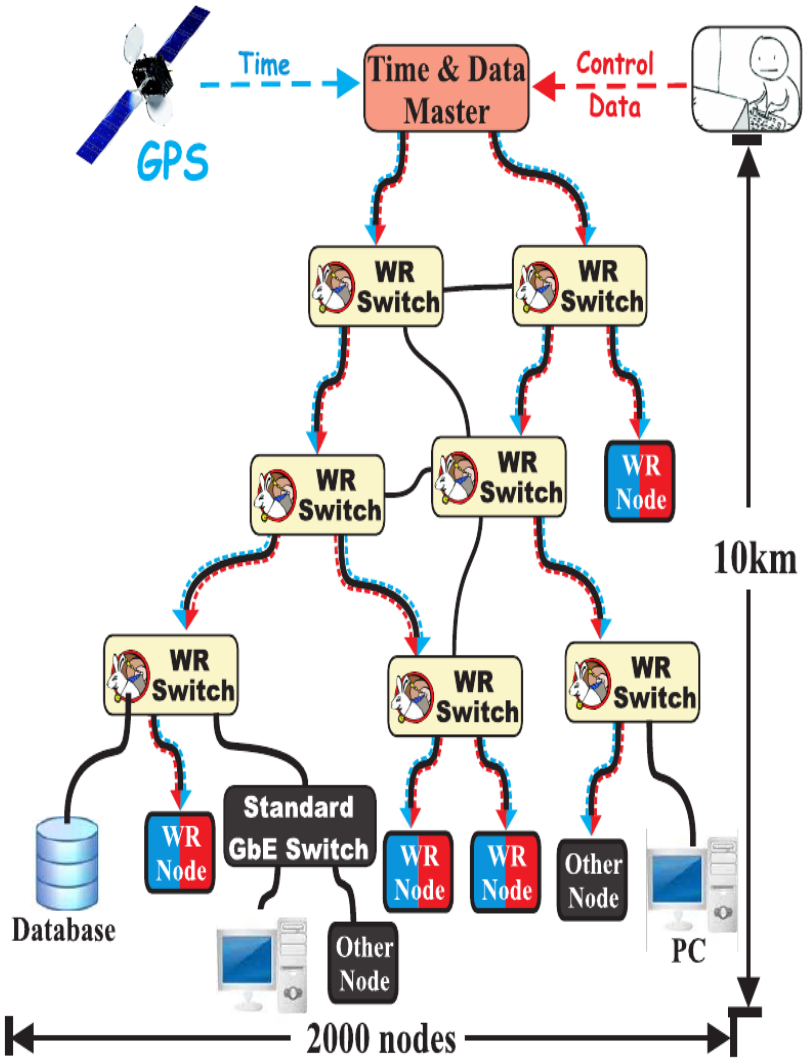


new architecture



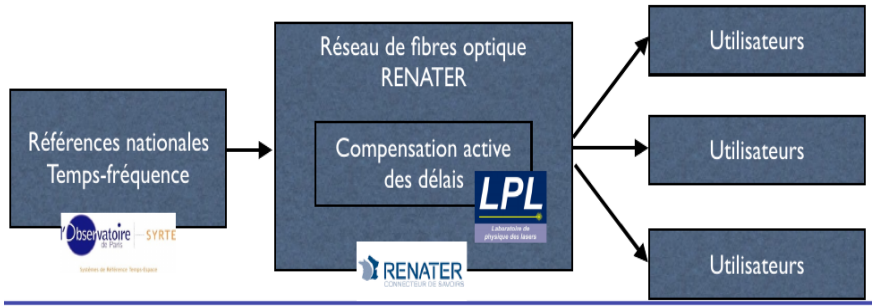
- new analog stage
- digitization at the antennas
- 500 MHz bandwidth, 14b 1Gsps ADC (2 channels)
- synchronization with White Rabbit
- fiber optics network

White Rabbit basics



- Extension of ethernet protocol for precise time distribution & deterministic latency
- all nodes have same clock frequency
- clock distributed over network
- uses PTP (Precision Time Protocol) for accurate latency determination (master⟷slave dialog over ethernet)
- and DDMTD for clock phase adjustment and tracking
- each node provide PPS and clock signals
- open hard-, firm- and software developped by CERN, NIKHEF, GSI,... (IEEE standard) ... now SAFRAN
- implemented (improved hardware) in IDROGEN board's design

Time & frequency distribution : T+REFIMEVE



- For long time stability reference clock is mandatory
- International time reference provider
- Optical fiber distribution

Signal provided by T-REFIMEVE		Stability @1s	Stability @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1st pillar - 10 MHz (White Rabbit)	10^{-12}	10^{-15}	10^{-14}	10^{-15}
	2nd pillar - 1 GHz	10^{-13}	3×10^{-16}	10^{-14}	2×10^{-16}
Time	1st pillar (White Rabbit)	1 ns	1 ns	10 ns	10 ns
	2nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps
Optical frequency (194,5 THz - 1542 nm)	Today	10^{-15}	3×10^{-16}	10^{-14}	2×10^{-17}
	Expected progress in 5 years	10^{-16}	2×10^{-17}	10^{-14}	10^{-18}

WhiteRabbit supervision

```
WR PTP Core Sync Monitor v 1.0
Esc = exit

TAI Time:                   Thu, Jan 1, 1970, 00:03:48

wru1: Link up   (RX: 685, TX: 281), mode: WR Slave   Locked  Calibrated
IPv4: BOOTP running

PTP status: slave

Synchronization status:

Servo state:                TRACK_PHASE
Phase tracking:             ON
Synchronization source:
Aux clock status:

Timing parameters:

Round-trip time (mu):    691831 ps
Master-slave delay:      349132 ps
Master PHY delays:       TX: 46407 ps, RX: 168643 ps
Slave PHY delays:        TX: 46407 ps, RX: 175043 ps
Total link asymmetry:       -6433 ps
Cable rtt delay:         255331 ps
Clock offset:                 0 ps
Phase setpoint:             528 ps
Skew:                         5 ps
Manual phase adjustment:      0 ps
Update counter:             174
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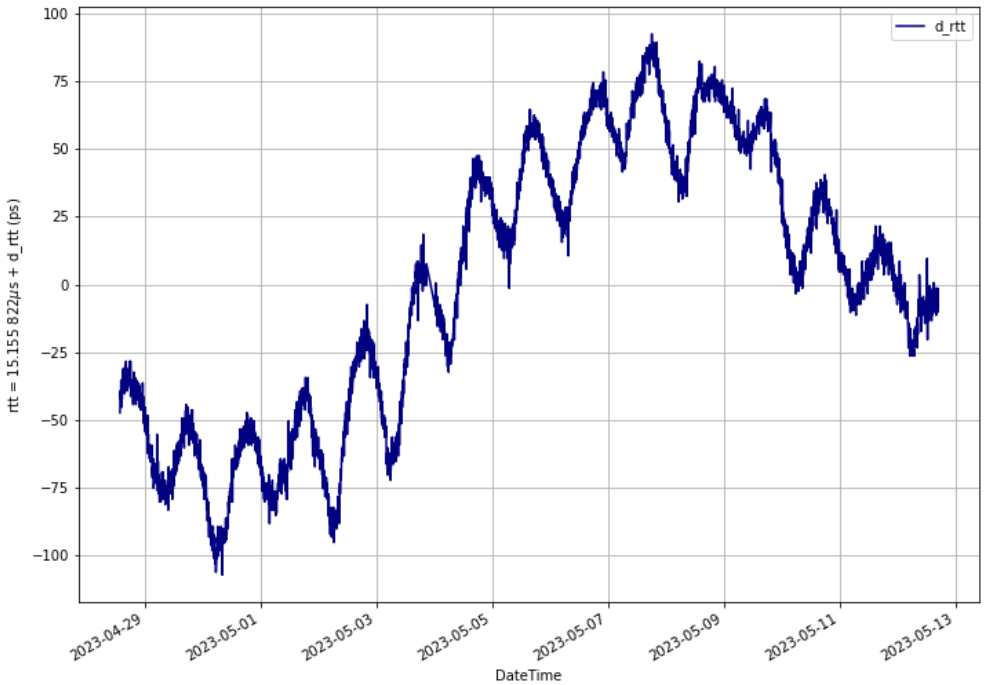
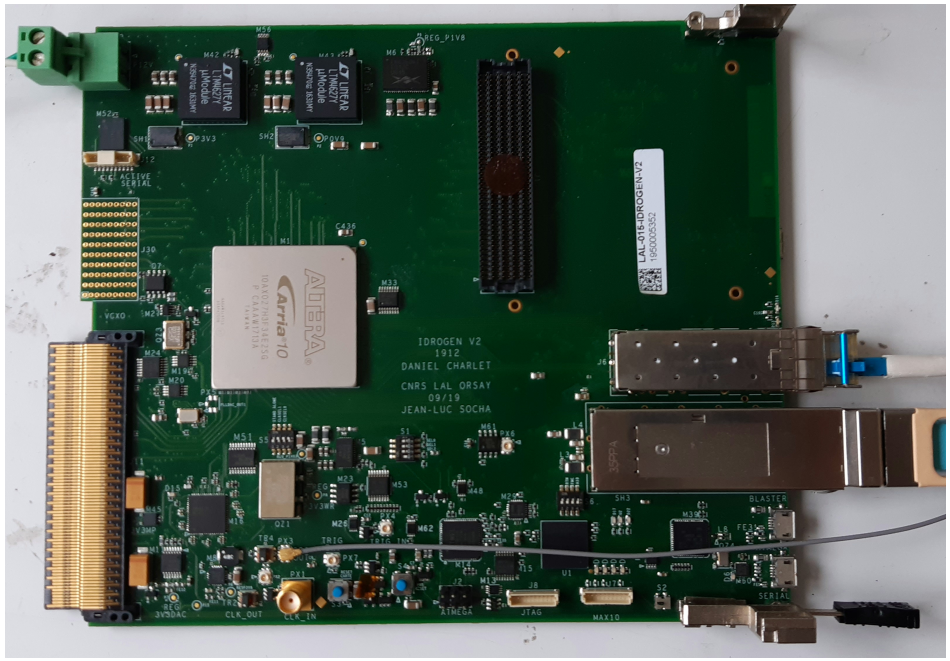


- WR debugging
  - Small operating system included in the WR core
  - Serial communication by USB or Ethernet
  - Status of the link : delays, transceiver
  - Control of the link : PPS,configuration
- WR supervision at LAC laboratory
- Monitoring at user equipment level
  - Fibers time propagation delays
  - 1.4Km of fiber
  - 5 levels of netwok stratum
  - 10 days of measurement
  - Zen-TP system

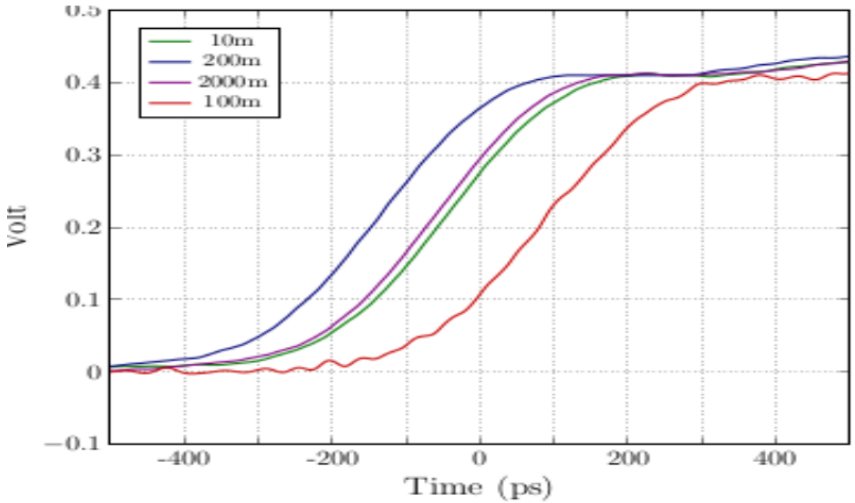
IDROGEN

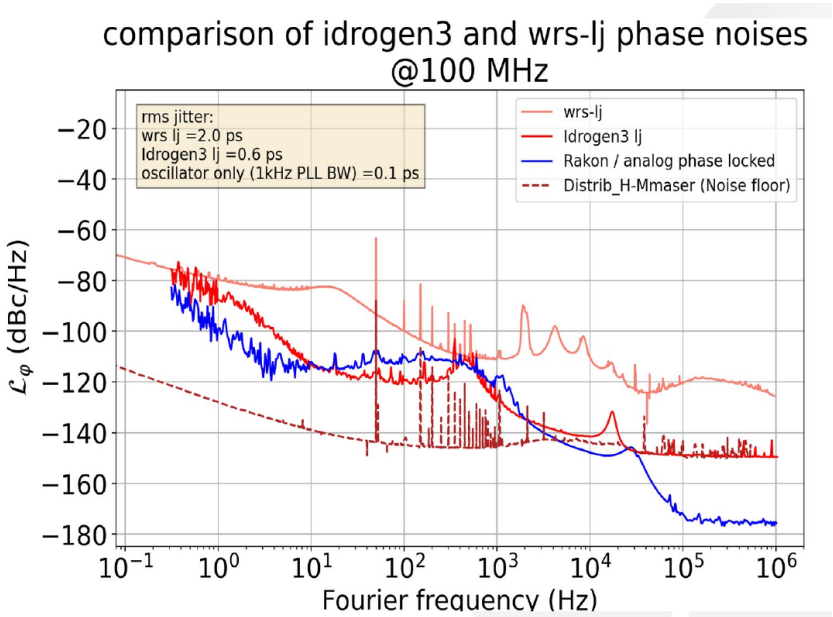
- generic acquisition board (DAQGEN IN2P3 program), IJCLab/SYRTE/Nançay collaboration
- Altera ARRIA 10 FPGA
- improved WR implementation
- additional mezzanine board (FMC connector) (several items under developments : ADC, timing, ...)
- optional MTCA (rack) connector (not for PAON4)
- connections :
  - USBs (FW upload, configuration, slow control)
  - 40gb QSFP+ (data + config/slow control)
  - 1Gb SFP+ (WR link)



WR with IDROGEN (SYRTE)

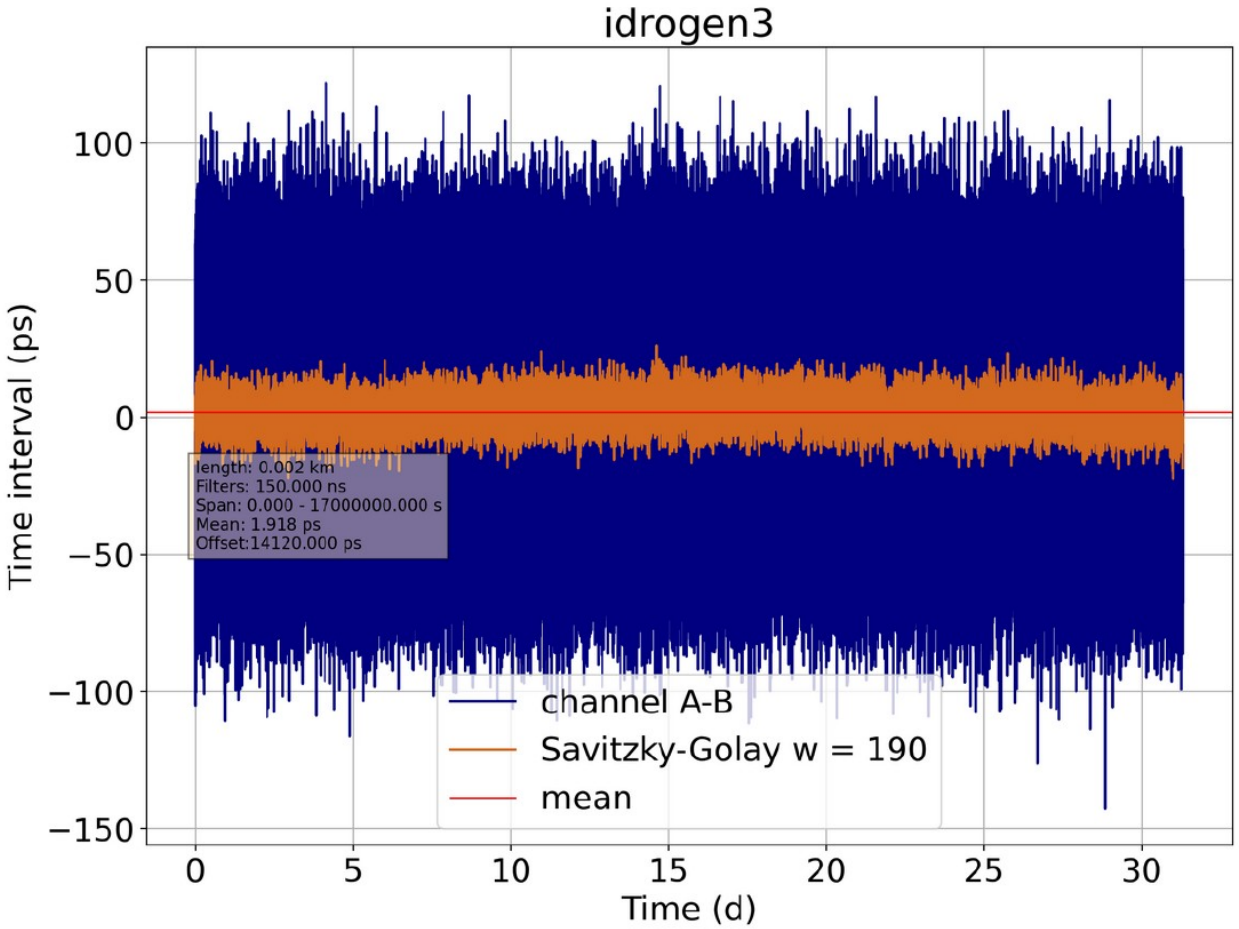
- qualification and calibration of IDROGEN boards WR parameters
- two boards, 10,100, 200 m, 2 km optical fiber link to WR switch (master)
  → ∼ 100 ps dispersion of PPS (preliminary WR params calibration)





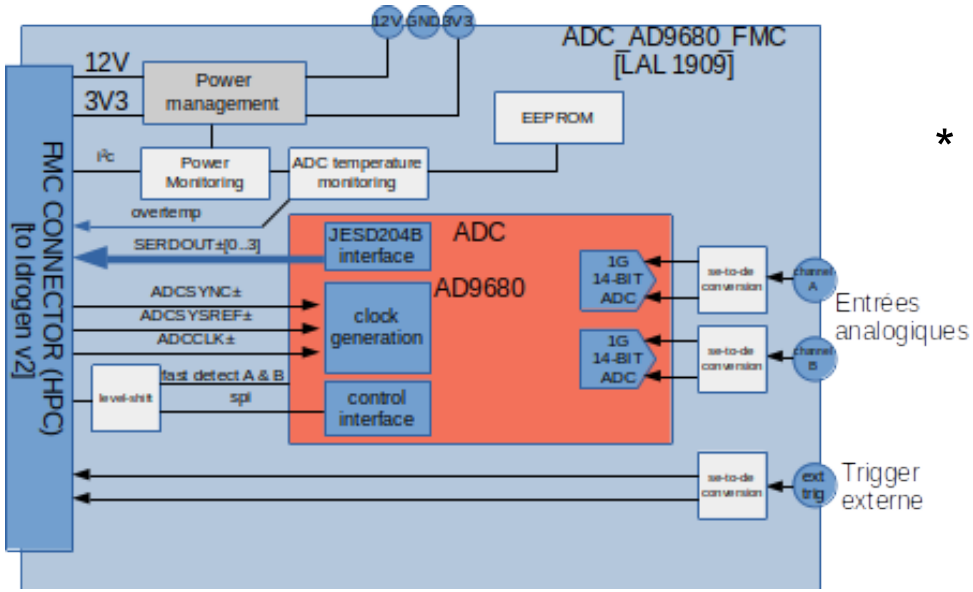
Idrogen WR stability (SYRTE)

PPS time difference between 2 Idrogen boards



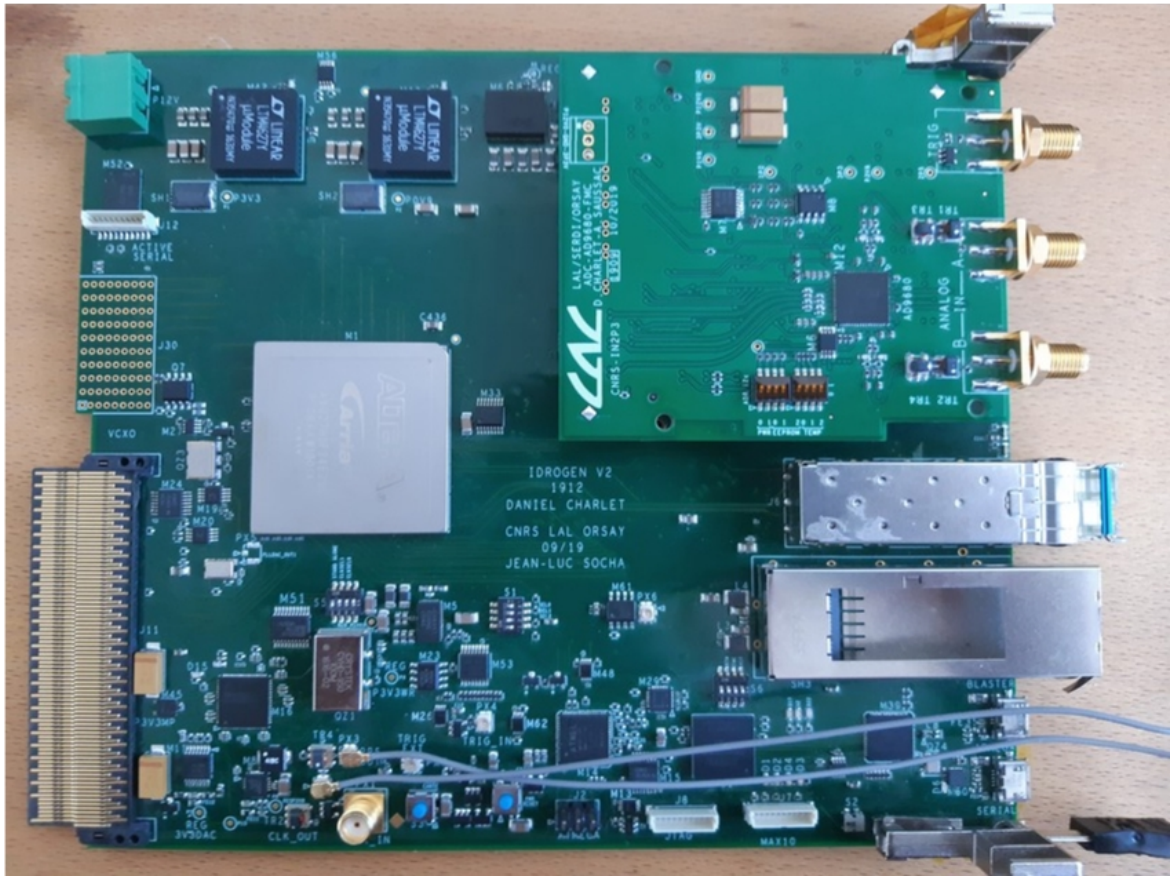
Excellent long term stability ; working on improving short term perfs

Mezzanine FMC ADC 1GSPS

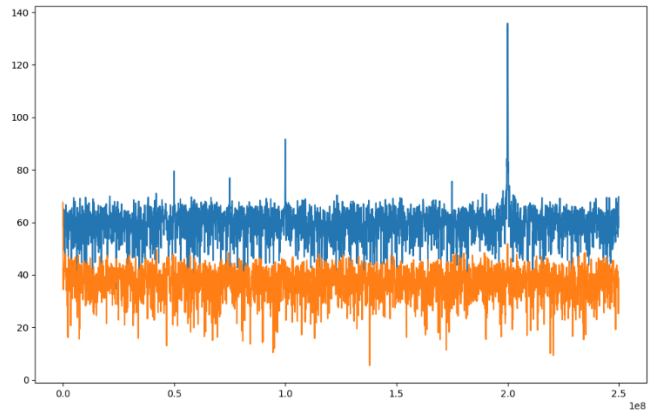


* The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :
  * includes : its own PLL.
  * ADC clock source : External clock
* Mezzanine main features :
  * VITA57.1 (FMC)
  * ADC 9680
  * 2 channels
  * 14 bits
  * 1 GSPS
  * JESD204
  * 2GHz analog bandwidth
  * External trigger in

IDROGEN + mezzanine FMC ADC 500MSPS



* Bandwidth 500 MHz to 1.5GHz
* Synchro & timing by WR
* Data transfer 2x 10G Ethernet
* Configuration by IPBus 10G
* ADC 1GSPS version currently in test

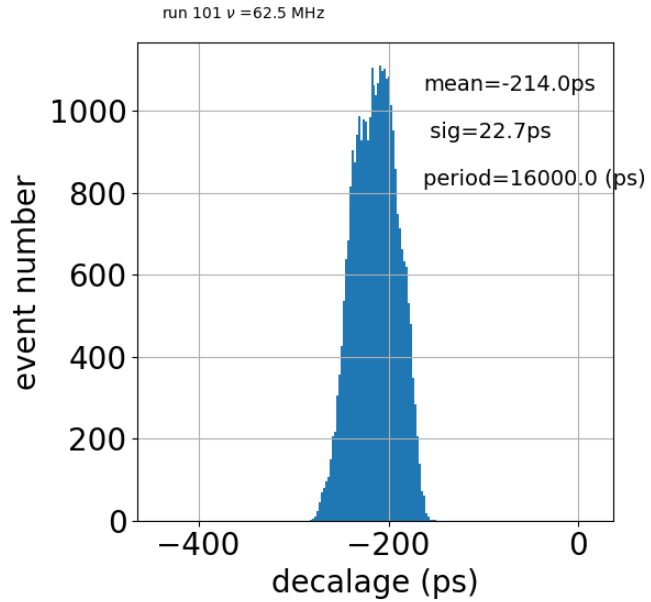


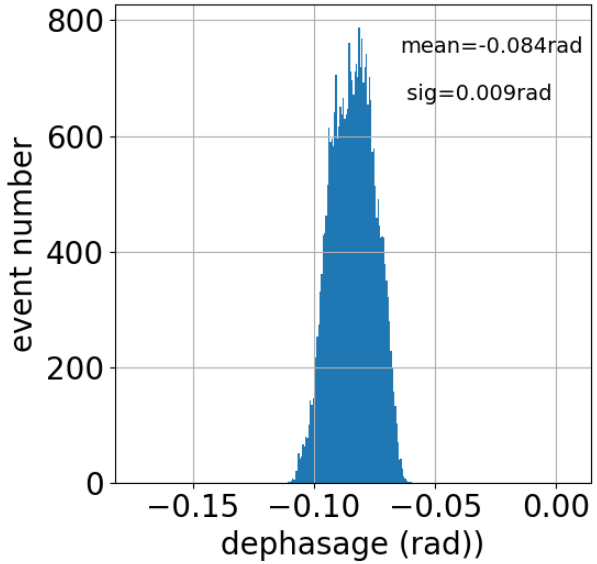
ADC samples timing checks (I)

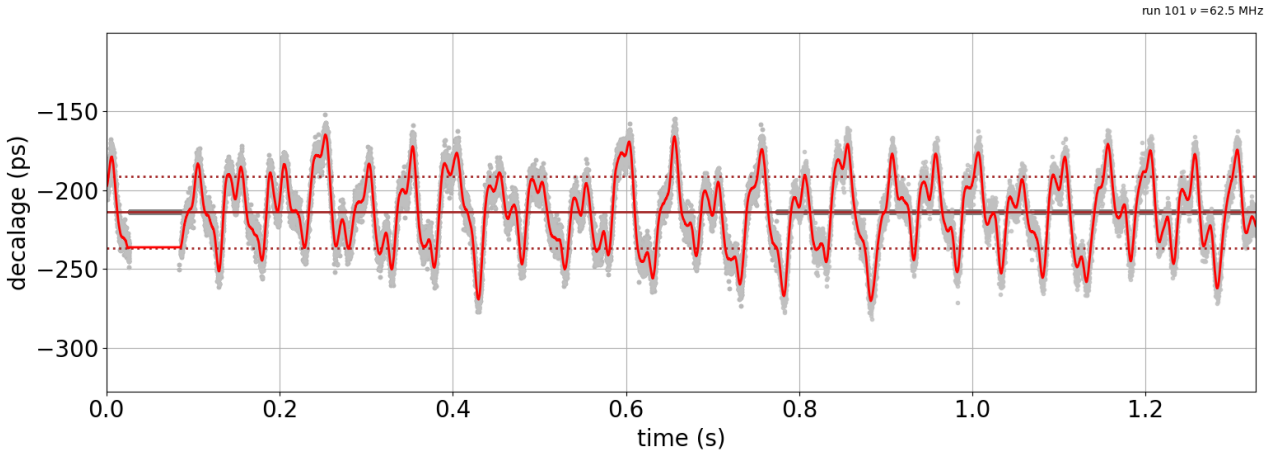
Basic setup :

- RF signal generator (pure sine wave, $\nu_0 = 62.5MHz$)
- two Idrogen + (prototype) mezzanine boards
- R/O of (16k samples) data chunks (events) with WR timestamps for a pair of channels
- FFT + x-correlation (if same timestamp)
- phase of ν_0 mode (1/chunk)
- $\phi(\nu_0) = 2\pi\delta t/T(\nu_0) = 2\pi\delta t\nu_0$ if timing difference δt between channels

Examples (PRELIMINARY)







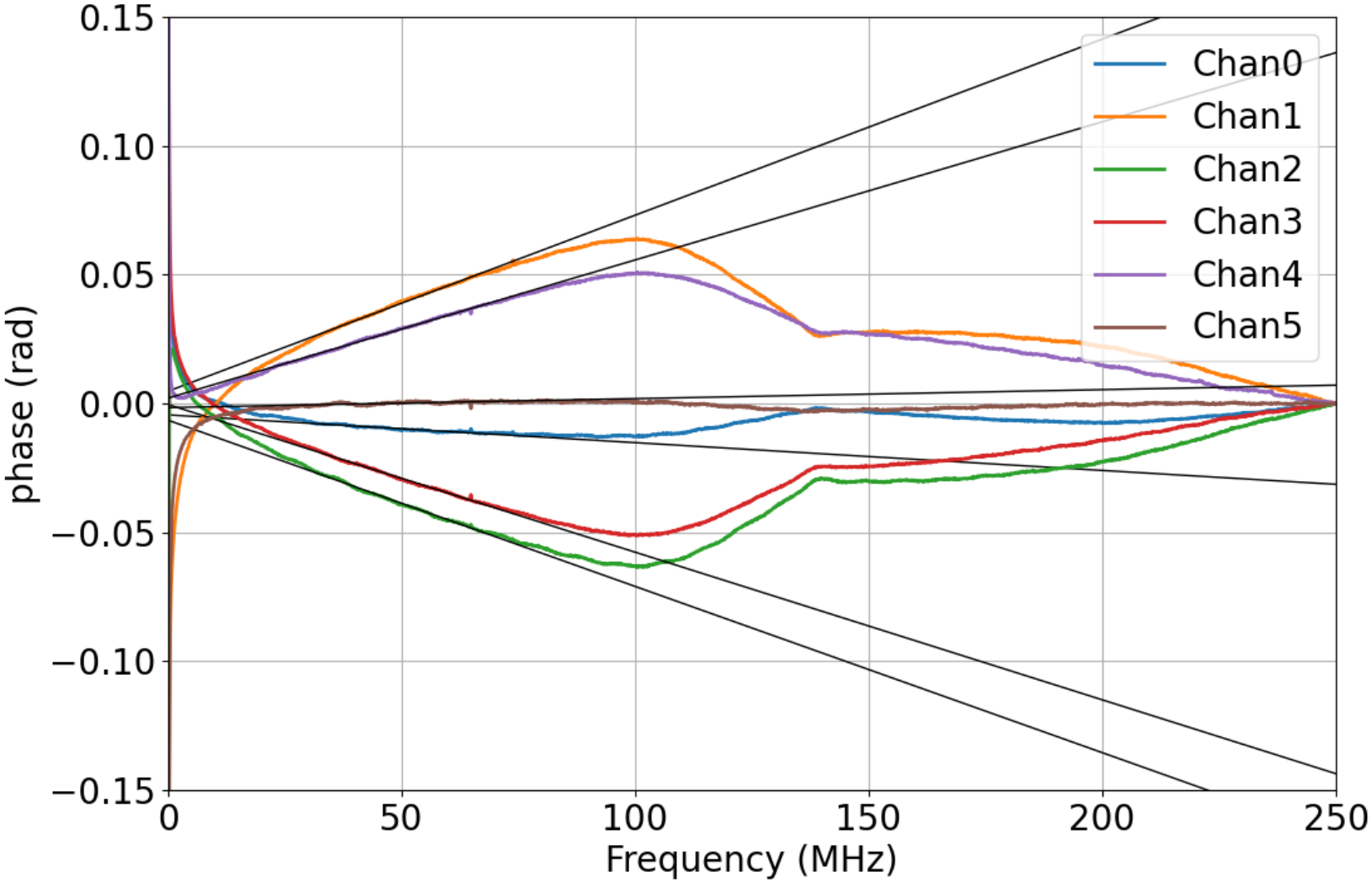
ADC samples timing checks (II)

Setup :

- RF white noise signal generator
- R/O of (8k samples) data chunks with WR timestamps for all (4) channels
- FFT + x-correlation (if same timestamp) of each chunk + time average
- $\phi(\nu) = 2\pi\delta t/T(\nu_0) = 2\pi\delta t\nu_0$ if timing difference δt between channels
- use phase vs frequency relation to check for δt
- Caveats :
  - use of prototype boards $\Rightarrow$ 500 Msps / 250 MHz bandwidth + broad low-pass filter at 250 MHz $\Rightarrow$ aliasing if $\nu \gtrsim 100$ MHz
  - setup unqualified at O(10 ps) timing accuracy

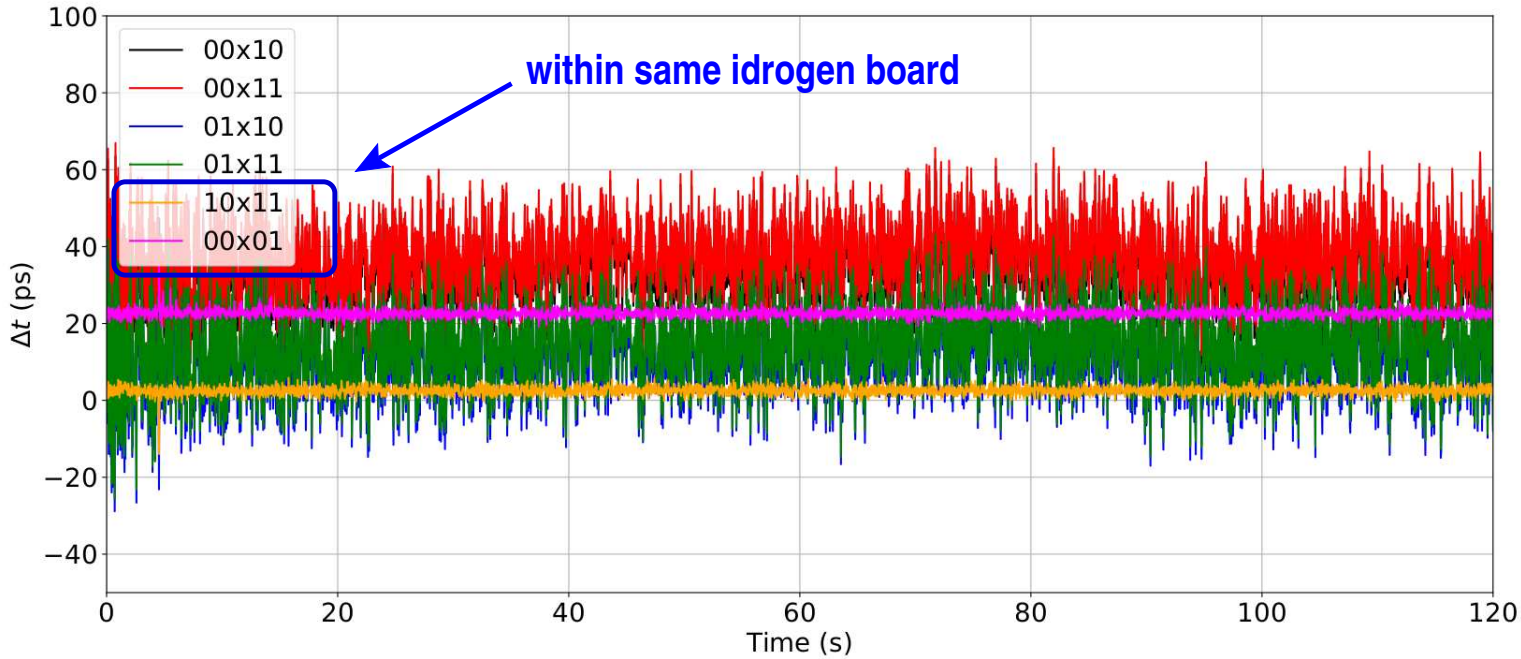
Some results (PRELIMINARY)

Time averaged phase vs frequency measurements



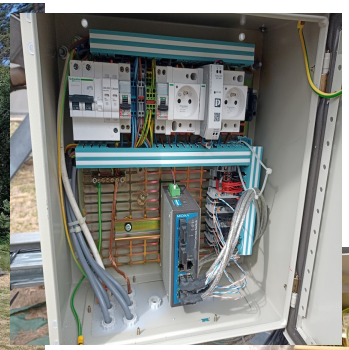
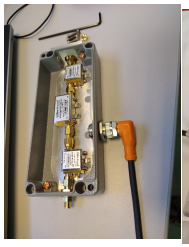
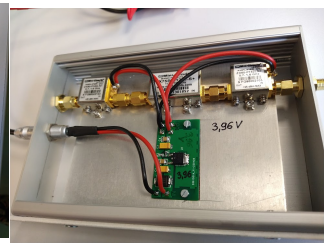
Latest results (PRELIMINARY)

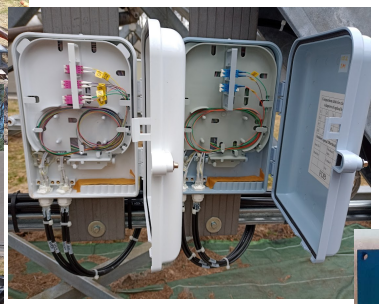
Averaged timing differences (in 40-70 MHz interval) vs time



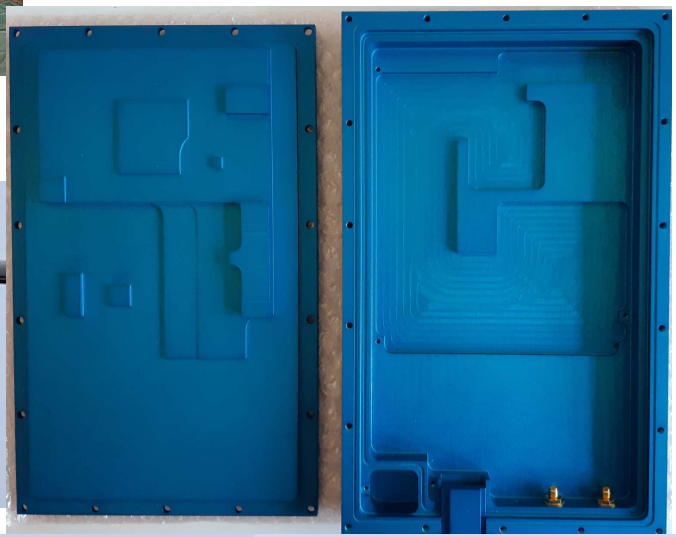
- channels from the same ADC : very stable (and small) timing diffference (setup ? board design ?)
- channels from different boards : averaged timing differences between boards of O(100 ps) (changes from one startup to the other) ⊕ O(50 ps) "fast" time variations (internal PLL ?)

Other developments (2022-2023)





Outlook

- Exploring a path toward 'on feed numerization'
- IDROGEN board :
  - generic acquisition board with WR implementation
  - applied in radio-astronomy for numerization on the antennas (+several other projects in HEP, NP, astro...)
  - UDP streamer for high data rate transmission OK
  - IPbus for configuration and slow control over ethernet OK
- WR timing performances ~ OK down to O(15 ps)
- other parts, including a new software correlator ~ ready
- ADC mezzanine for PAON4 :
  - firmware (ADC R/O, WR timing and data transmission over UDP link) seems OK with 500 Ms/s ADC
  - promising timing perfs, startup scheme under study to improve reproducibility & stability
  - Tests of nominal ADC (1 Gs/s) will begin after summer break
- integration tests and operations on the sky with PAON4 soon (with fingers crossed !)